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PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : **H01R 9/09** | **A1**

(11) International Publication Number: **WO 00/16443**

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(21) International Application Number: PCT/US99/20418

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60/099,730 10 September 1998 (10.09.98) US

(63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application
US 60/099,730 (CIP)
Filed on 10 September 1998 (10.09.98)

(71) Applicant *(for all designated States except US)*: VIASYSTEMS GROUP, INC. [US/US]; Suite 400, 101 South Hanley Road, St. Louis, MO 63105 (US).

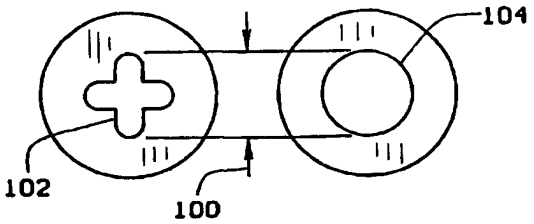
(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: COTTON, Martin, A. [GB/GB]; Eldon Street, South Shields, Tyne & Wear NE33 5BU (GB).

(74) Agent: EVANS, Lawrence, E., Jr.; Herzog, Crebs & McGhee, LLP, One City Centre, 24th floor, 515 North Sixth Street, St. Louis, MO 63101-2409 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: NON-CIRCULAR MICRO-VIA



(57) Abstract

Non-circular micro-vias (102) for printed circuit boards are disclosed and a method of making them.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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09/786787

RECEIVED
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PATENT COOPERATION TREATY

PCT

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To: LAWRENCE E. EVANS, JR.
HERZOG, CREBS & MCGHEE, LLP
ONE CITY CENTRE, 24TH FLOOR
515 NORTH SIXTH STREET
ST. LOUIS MO 63101-2409

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	19 OCT 2000
Applicant's or agent's file reference: 5687-009	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority Date *(day/month/year)*
PCT/US99/20418	07 SEPTEMBER 1999	10 SEPTEMBER 1998

Applicant
VIASYSTEMS GROUP, INC.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	KAMAND CUNEO
Facsimile No. (703) 305-3230	Telephone No. (703) 308-1233

Form PCT/IPEA/416 (July 1992)★

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 5687-009	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/US99/20418	International filing date *(day/month/year)* 07 SEPTEMBER 1999	Priority date *(day/month/year)* 10 SEPTEMBER 1998
International Patent Classification (IPC) or national classification and IPC IPC(7): H01R 12/04 and US Cl.: 174/262		
Applicant VIASYSTEMS GROUP, INC.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 0 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report

   II ☐ Priority

   III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability

   IV ☐ Lack of unity of invention

   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   VI ☐ Certain documents cited

   VII ☐ Certain defects in the international application

   VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
13 MARCH 2000	14 SEPTEMBER 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer USPTO KAMAND CUNEO Telephone No. (703) 308-1233

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/20418

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-19 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the claims:
pages 20-33 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the drawings:
pages 1-4 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages none

[X] the claims, Nos. none

[X] the drawings, sheets/~~fig~~ none

5. [X] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/20418

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-26	YES
	Claims	none	NO
Inventive Step (IS)	Claims	1-26	YES
	Claims	none	NO
Industrial Applicability (IA)	Claims	1-26	YES
	Claims	none	NO

2. citations and explanations (Rule 70.7)

Claims 1-26 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest the following.The Sen et al. reference which is indicated as disclosing the claims with the convoluted through hole does not teach the the claimed combination with the through hole being plated.

---------- NEW CITATIONS ----------
NONE

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

5. (Some) amendments are considered to go beyond the disclosure as filed:
NONE

PATENT COOPERATION TREATY 09/786787/15

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

REC'D 25 OCT 2000
WIPO PCT

Applicant's or agent's file reference 5687-009	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US99/20418	International filing date *(day/month/year)* 07 SEPTEMBER 1999	Priority date *(day/month/year)* 10 SEPTEMBER 1998
International Patent Classification (IPC) or national classification and IPC IPC(7): H01R 12/04 and US Cl.: 174/262		
Applicant VIASYSTEMS GROUP, INC.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 0 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report

   II ☐ Priority

   III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability

   IV ☐ Lack of unity of invention

   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   VI ☐ Certain documents cited

   VII ☐ Certain defects in the international application

   VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
13 MARCH 2000	14 SEPTEMBER 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer USPTO KAMAND CUNEO Telephone No. (703) 308-1233

Form PCT/IPEA/409 (cover sheet) (July 1998)★

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/20418

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-19 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the claims:
pages 20-33 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the drawings:
pages 1-4 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages none

[X] the claims, Nos. none

[X] the drawings, sheets~~/fig~~ none

5. [X] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/20418

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-26	YES
	Claims	none	NO
Inventive Step (IS)	Claims	1-26	YES
	Claims	none	NO
Industrial Applicability (IA)	Claims	1-26	YES
	Claims	none	NO

2. citations and explanations (Rule 70.7)

Claims 1-26 meet the criteria set out in PCT Article 33(2)-(4), because the prior art does not teach or fairly suggest the following.The Sen et al. reference which is indicated as disclosing the claims with the convoluted through hole does not teach the the claimed combination with the through hole being plated.

---------- NEW CITATIONS ----------
NONE

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

I. BASIS OF REPORT:

5. (Some) amendments are considered to go beyond the disclosure as filed:
NONE

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

09/786787

DEC 10

PCT

sme

To: LAWRENCE E. EVANS, JR.
HERZOG, CREBS & MCGHEE, LLP
ONE CITY CENTRE, 24TH FLOOR
515 NORTH SIXTH STREET
ST. LOUIS MO 63101-2409

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

	Date of Mailing *(day/month/year)* 02 DEC 1999
Applicant's or agent's file reference 5687-009	FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/US99/20418	International filing date *(day/month/year)* 07 SEPTEMBER 1999
Applicant VIASYSTEMS GROUP, INC.	

1. [X] The applicant is hereby notified that the international search report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the international search report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

[ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

[ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after 18 months from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in rules 90 *bis* 1 and 90 *bis* 3, respectively, before the completion of the technical preparations for international publication.

Within 19 months from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within 20 months from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer KAMAND CUNEO
Facsimile No. (703) 305-3230	Telephone No. (703) 308-1233

PATENT COOPERATION TRE Y

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 5687-009	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
International application No. PCT/US99/20418	International filing date *(day/month/year)* 07 SEPTEMBER 1999	(Earliest) Priority Date *(day/month/year)* 10 SEPTEMBER 1998
Applicant VIASYSTEMS GROUP, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (See Box I).

2. [ ] **Unity of invention is lacking** (See Box II).

3. [ ] The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
   - [ ] filed with the international application.
   - [ ] furnished by the applicant separately from the international application,
     - [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
   - [ ] transcribed by this Authority.

4. With regard to the **title**,
   - [X] the text is approved as submitted by the applicant.
   - [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   - [ ] the text is approved as submitted by the applicant.
   - [X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is:

   Figure No. 1
   - [X] as suggested by the applicant.
   - [ ] because the applicant failed to suggest a figure.
   - [ ] because this figure better characterizes the invention.
   - [ ] None of the figures.

ernational application No.
PCT/US99/20418

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

Non-cicular micro vias (102) for printed circuit boards are disclosed and a method of making them.

INTERNATION[illegible] SEARCH REPORT

[illegible]rnational application No.
[illegible]CT/US99/20418

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01R 9/09
US CL :174/262

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/262, 260, 261, 264, 265, 35R, 255

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 5,414,222 A (SEN et al.) 09 MAY 1995, (09/05/95) FIGS 2-3F	1,7, 8, 3-16,17-19 ---------- 3-4
Y	US 5,522,132 A (MATTEI) 04 JUNE 1996, (04/06/96) FIG 5	5
Y	US 5,734,560 A (KAMPERMAN et al.) 31 MARCH 1998, (3F1/03/98) IGS 1-2	3-4
A	US 5347086 A (POTTER et al.) 13 SEPTEMBER 1994, (13/09/94) FIG 3	6
A	US 5,442,144 A (CHEN et al.) 15 AUGUST 1995, (15/08/95) FIG 1	3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 16 NOVEMBER 1999	Date of mailing of the international search report 02 DEC 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KAMAND CUNEO Telephone No. (703) 308-1233

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under Article 19. The Notes are based on the requirements of the Patent Cooperation Treaty and of the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule" and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the international application may be amended ?

The claims only.

The description and the drawings may only be amended during international preliminary examination under Chapter II.

When ? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments ?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How ? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 205(b)).

What documents must/may accompany the amendments ?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confounded with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped), whether

(i) the claim is unchanged;
(ii) the claim is cancelled;
(iii) the claim is new;
(iv) the claim replaces one or more claims as filed;
(v) the claim is the result of the division of a claim as filed.

US005414222A

United States Patent [19]

Sen et al.

[11] Patent Number: 5,414,222

[45] Date of Patent: May 9, 1995

[54] **MULTILAYER IC SEMICONDUCTOR PACKAGE**

[75] Inventors: **Bidyut K. Sen**, Milpitas; **Eric S. Tosaya**, Fremont, both of Calif.

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: **108,029**

[22] Filed: **Aug. 17, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 881,955, May 12, 1992, Pat. No. 5,304,743.

[51] **Int. Cl.**[6] **H05K 1/00**

[52] **U.S. Cl.** **174/262**; 361/784; 174/263; 174/265

[58] **Field of Search** 174/262, 263, 264, 265, 174/266; 361/784, 792

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Primary Examiner—Leo P. Picard
Assistant Examiner—Cheryl R. Figlin
Attorney, Agent, or Firm—Townsend and Townsend Khourie and Crew

[57] **ABSTRACT**

An improved multilayer integrated circuit package. The package, which has a plurality of layers of conducting leads, has metal vias which connects leads in a first layer connected to leads in a second layer. The improvement comprises having at least on of the vias with a cross-section such that the via is much larger in a first direction than in a second direction generally perpendicular to the first direction.

4 Claims, 2 Drawing Sheets

Relevant

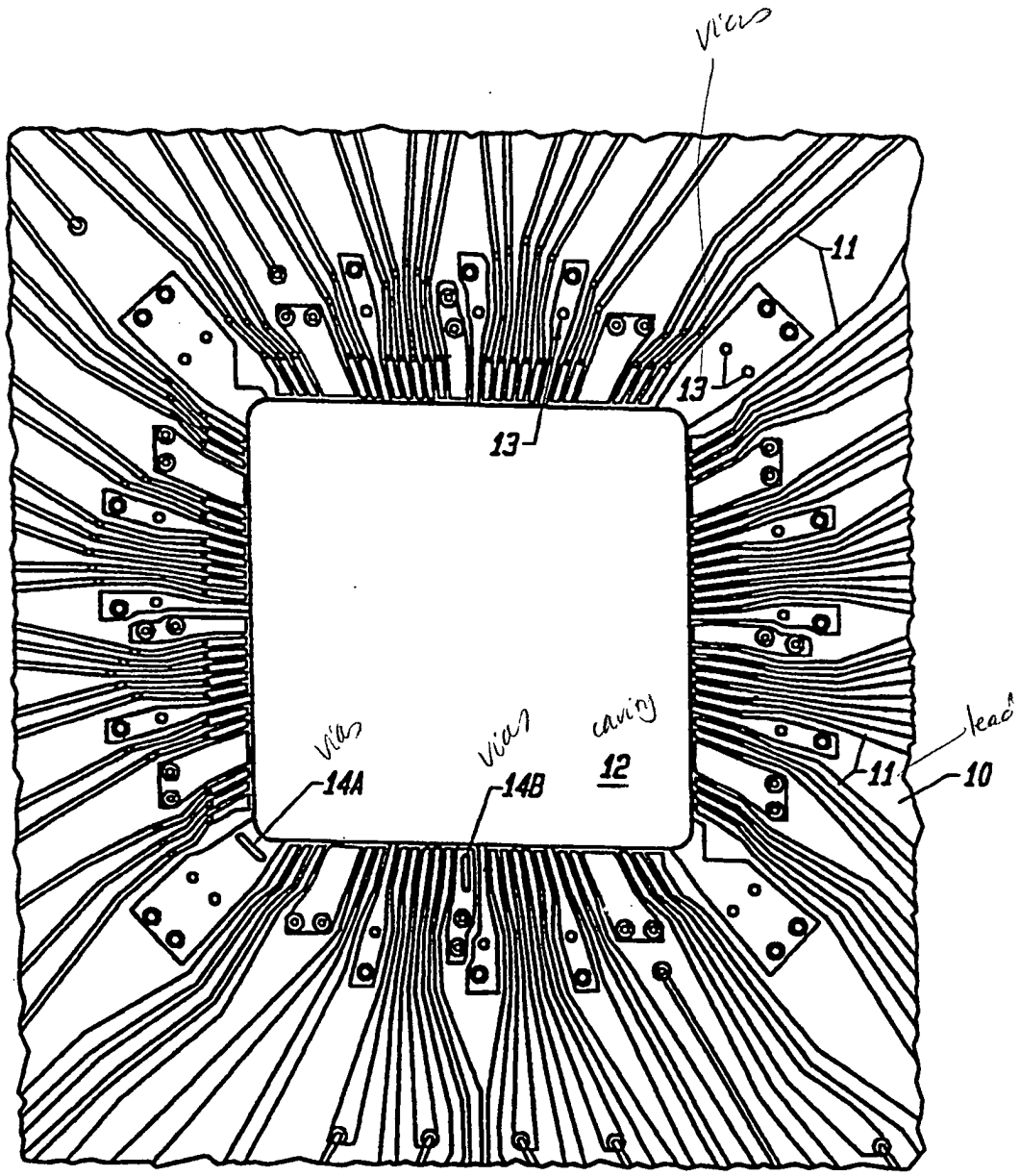

FIG. 1

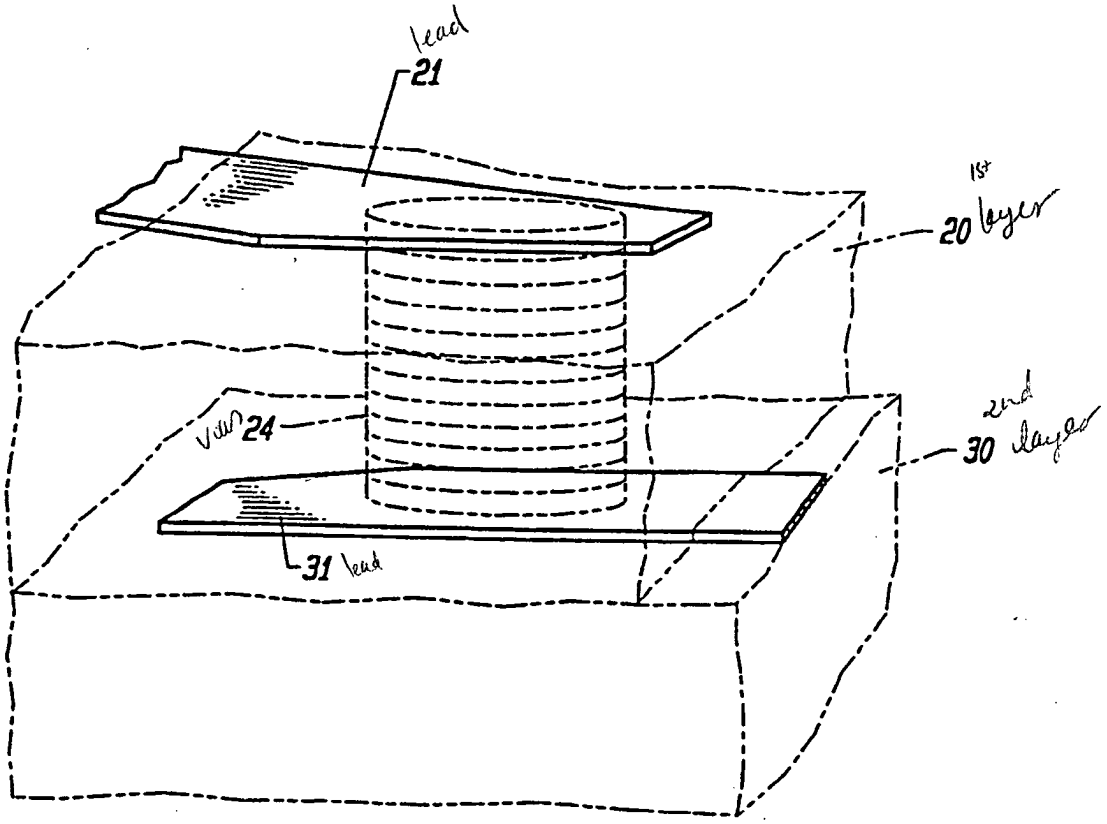

FIG. 2

FIG. 3A

FIG. 3D

FIG. 3B

FIG. 3E

FIG. 3C

FIG. 3F

MULTILAYER IC SEMICONDUCTOR PACKAGE

This is a continuation of Ser. No. 881,955, filed May 12, 1992, now U.S. Pat. 5,304,743.

BACKGROUND OF THE INVENTION

This patent application is related to packaging of integrated circuits and, more specifically, to multilayer integrated circuit packaging.

After the processing of a semiconductor wafer is complete, the individual integrated circuit units, or die, are separated and encased in some form of packaging so that the integrated circuit can be safely handled and mounted in an electrical system. The integrated circuit package has conducting wire leads which are connected by wires to bonding pads on the integrated circuit in the interior of the package. Connected to the outside of the package, the wire leads provide a path for communicating with the encased integrated circuit.

Among the various types of packages are multilayer packages. Such packages are useful for integrated circuits having a large number of bonding pads and therefore requiring a large of number of conducting leads. Such integrated circuits include microprocessors, gate array, and other kinds of ASICs (Application Specific Integrated Circuit), which therefore require a large number of conducting leads.

A common problem in semiconductor packaging technology is the noise generated by simultaneously switching signals, such as those on a data bus, by the adjacent leads. For example, it is common that the amount of current in a lead to rise or drop 75 milliamperes in magnitude within 1 nanosecond. With parasitic inductive coupling, particularly between power/-ground leads and adjacent leads, signal switching on one lead can cause spurious voltages, i.e., noise, to be generated on the adjacent leads of the package. These spurious voltages lead to the sensing of erroneous signals on the adjacent leads.

Various solutions have long been sought to avoid these problems. Among the solutions have been the design of the integrated circuit to slow down the slew rate of the driver circuits to avoid deleterious noise from outgoing signals from the integrated circuit. However, this is not an optimal solution because the integrated circuit is slowed. Generally the faster the operation of an electrical system, the better the system.

Other solutions have included reducing the number of simultaneously switching output signals, increasing the distance between switching leads, providing more power and ground pins, adding large "deadpanning" capacitors, deskewing the switching bus and so forth.

On the other hand, the present invention solves or substantially mitigates this problem without any of these drawbacks and permits the integrated circuit in its package to operate effectively at high switching speeds.

SUMMARY OF THE INVENTION

The present invention provides for an improved multilayer integrated circuit package. The package, which has a plurality of layers of conducting leads, has metal vias which connects leads in a first layer connected to leads in a second layer. The improvement comprises having at least one of the vias with a cross-section such that the via is much larger in a first direction than in a second direction generally perpendicular to said first direction.

BRIEF DESCRIPTION OF THE DRAWINGS

A more detailed understanding of the present invention may be attained by a perusal of the following Detailed Description of Preferred embodiment(s) with reference to the following drawings:

FIG. 1 is a top view of a portion of a single layer in multilayer integrated circuit package.

FIG. 2 is an idealized prospective view of a via connecting two leads on separate layers of a multilayer package.

FIGS. 3A–3F are cross-sectional top views of vias according to various embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT(S)

FIG. 1 is a top view of a portion of an exemplary single layer of a multilayer integrated circuit package. Typically these layers are made from ceramic material with different conducting metallic materials formed on the ceramic layer. The multilayer package typically has two or more of these layers with conducting leads sandwiched between a top and bottom layer to complete the package.

However, it should be noted that this invention is not limited to ceramic packaging only, but is applicable to packaging using thick and thin films, PCB materials such as FR4, polyimides such as Kapton and Upiplex, and other combinations of dielectric and conducting materials.

As shown in FIG. 1, a multitude of conducting leads 11 on a ceramic substrate 10 surround a central cavity 12. The cavity 12 receives an integrated circuit and wire leads are bonded between the ends of the conducting leads 11 and the bonding pads on the integrated circuit. The conducting leads 11 lead to the exterior of the package. Again, it should be noted that the present invention is not limited to wire bonding, but is equally applicable to TAB, flip-chip, and other types of die-to-package interconnects.

As can be seen in FIG. 1, the leads 11 are tightly packed around the cavity 12. Hence additional leads on other ceramic layers are used to provide access for electrical signals to and from the integrated circuit. The conducting leads on different layers are connected by vias through the ceramic material. Heretofore these vias have been circular or square in cross-section. Such circular vias are shown by vias 13. For conducting leads which carry large currents, multiple parallel-connected vias in close proximity are used to reduce the current density through each via. Such multiple parallel-connected vias are in FIG. 1 by vias 15. Of course, to reduce the complexity of the drawing, it should be noted that not all of the via 13 and 15 are shown in FIG. 1.

However, while reducing the problem of current density and increased path resistance, the parallel-connected vias still have the problems faced by single vias, i.e., large parasitic inductances. Moreover, the parallel-connected vias offer increased capacitance thereby slowing signals on the paths.

In contrast, the present invention uses vias which have relatively low parasitic inductances and resistances. FIG. 1 shows two vias 14A and 14B according to the present invention. Via 14A is placed such that, in a cross-sectional view, its long axis is generally perpendicular to the longitudinal axis of the conducting lead,

while via 14B has its cross-sectional long axis generally perpendicular with the axis of the conducting lead.

In accordance with the present invention, vias, as seen in a cross-sectional top view, are much larger in one direction compared to a direction perpendicular to the first direction. This allows each via to have a large total cross-sectional area to lower the impedance of the via, while insuring that no voids are created in the via during the manufacturing process of the package. In ceramic packaging, for example, vias are formed in through-holes in an intermediate ceramic sheet to connect leads on different ceramic sheets. The through-hole is filled with a paste from a metal, such as tungsten. Then the ceramic sheet is fired, along with the rest of the package. If the through-hole is too large, undesirable voids are formed in the resulting metal via after firing. With the present invention, the shorter axis of the via cross-section in a ceramic package is kept at less than 10 mils. This ensures that the through-hole is properly filled by the metallic paste and no voids are formed in the via. The via is solid.

FIG. 2 illustrates a via according to the present invention. A via 24 having an elongated oval cross-section connects a lead 21 on a layer 20 to a lead 31 on a second layer 30. Each lead 21 and 31 is part of a large number of leads formed respectively on the layers 20 and 30. The via 24 is formed through the layer 20. Besides two leads, a via in accordance with the present invention could connect two conducting planes, or a lead and a plane on separate layers equally well.

With the large cross-sectional area, a via according to the present invention has a lower resistance than a standard via. Contact resistance, i.e., resistance of the interface between the via and the lead, is also lowered. Compared to parallel-connected vias, a via according to the present invention has a much lower capacitance. These improvements lower the parasitic RC time constants for faster signal switching speeds.

Furthermore, a via in accordance with the present invention reduces parasitic inductance. The via shape allows the via to be placed much closer to the end of a lead, such as those for power and ground, compared to multiple parallel-connected vias. This shortening of lead lengths reduces inductance which permits an integrated circuit package with higher performance. With the reduction in the inductance of the power and ground leads, for example, the ground bounce immunity of the package improves. The package is able to handle a greater number of switching outputs, or stated differently, does not require as many power and ground pins. More powerful or faster output buffers may be supported in the package.

Finally, besides lower parasitic inductance, lower resistance through the via, lower contact resistance, the present invention provides for better shielding, or isolation, of the conducting leads in the package. In multilayer packages many of the layers are formed from power and ground planes to provide various access to power and ground. It is desirable that the power planes be connected together by large connections to handle the heavy currents through these planes generated by the signal switching of the packaged integrated circuit in as many locations as possible. This is also true for the ground planes with connections passing through holes in the vias of opposite type.

With large circular and square vias, it is difficult to make these connections at as many and specific locations as desired. With vias according to the present invention, on the other hand, these connections can be conveniently made at desired locations. These connections provide shielding for the signals on the leads 11, which are located on layers between the power and ground plane layers.

This shielding of signals can be seen from a side cross-sectional view of the package, which intersects any two planar connections. From this view any leads between the planar connections appear to be surrounded by a continuous band of conducting material. In other words, in a side cross-sectional view, the leads appear to form part of a coaxial cable. Thus the leads are shielded. Furthermore, the vias according to the present invention have long axes which may be aligned to enhance the effect of a coaxial cable.

FIGS. 3A–3F illustrate various cross-sectional top views of vias according, to the present invention. The via in FIG. 3A is simply a long rectangle. The FIG. 3B via is a long oblong. In FIG. 3C the via is a series of interconnected circles. This shape allows the circular punch which is presently used to create vias to be used. The FIG. 3D via is a series of interconnected rectangles of different sizes. The rectangles are generally aligned along their long axes. This shape allows two differently sized rectangular punches to be used to create vias according to the present invention. In FIG. 3E the via is a series of circles interconnected by rectangles. As in the via of FIG. 3D the interconnecting rectangles are generally aligned along their long axes. This is also true for the via illustrated in FIG. 3F. The interconnecting rectangles link is a series of oblongs which also have their long axes generally aligned with the axes of the rectangles.

While the above is a complete description of the preferred embodiments of the invention, various alternatives, modifications and equivalents may be used. It should be evident that the present invention is equally applicable by making appropriate modifications to the embodiments described above. Therefore, the above description should not be taken as limiting the scope of the invention which is defined by the metes and bounds of the appended claims.

What is claimed is:

1. An improved multilayer integrated circuit package, said package having a plurality of layers of conducting leads, at least one of said leads in a first layer connected to a lead in a second layer by a metal via, the improvement comprising said via having a cross-section such that said via is much larger in a first direction than in a second direction perpendicular to said first direction.

2. The improved multilayer integrated circuit as in claim 1 wherein said via cross-section is in the shape of an elongated oval.

3. The improved multilayer integrated circuit as in claim 1 wherein said via cross-section is in the shape of an elongated rectangle.

4. The improved multilayer integrated circuit as in claim 1 wherein said via cross-section is no more than 10 mils in said second direction.

* * * * *

US005522132A

United States Patent [19]

Mattei

[11] Patent Number: 5,522,132

[45] Date of Patent: Jun. 4, 1996

[54] MICROWAVE SURFACE MOUNT PACKAGE

[75] Inventor: Carmelo J. Mattei, Phoenix, Ariz.

[73] Assignee: St Microwave Corp., Arizona Operations, Chandler, Ariz.

[21] Appl. No.: 346,523

[22] Filed: Nov. 29, 1994

Related U.S. Application Data

[62] Division of Ser. No. 72,819, Jun. 7, 1993, Pat. No. 5,401,912.

[51] Int. Cl.[6] H05K 3/02

[52] U.S. Cl. 29/846; 174/262; 257/728

[58] Field of Search ..... 174/250, 255, 174/262, 263, 264, 265, 266, 35 R, 35 GC, 52.1–52.4; 361/794, 813, 816, 818; 428/901; 29/825, 829, 846, 843; 257/728, 774

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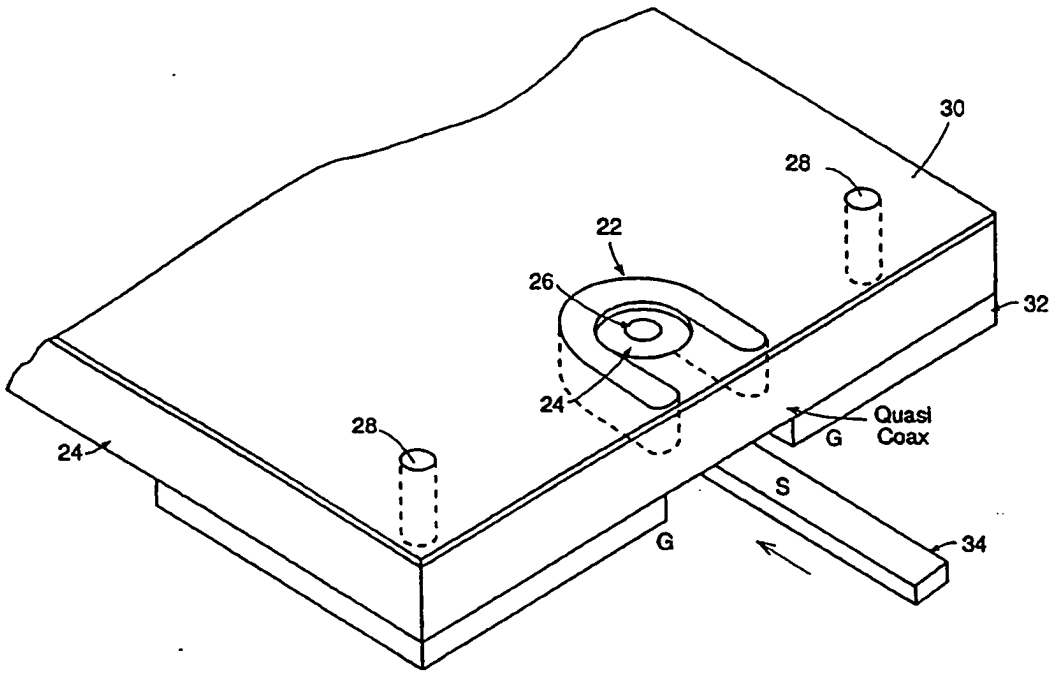
Robert J. DeBoo et al. *New Surface-Mounted Package Breaks from Traditional MIC Packaging*, Microwave Journal, Mar. 1984.

Primary Examiner—Kristine L. Kincaid
Assistant Examiner—Christopher Horgan
Attorney, Agent, or Firm—Bryan Cave; David M. Klein

[57] ABSTRACT

An improved surface mount package and method of making such a package is provided. A conventional surface mount package is modified by fabricating a U-shaped via around the lead via to form a quasi-coaxial transmission line through the insulating substrate. This permits the electrical impedance in the conductive elements of the surface mount package to be controlled to reduce insertion loss and return loss, and to improve isolation. The surface mount package includes a lead frame, and a gold plate to which an integrated circuit in the package is attached. The package is sealed with a ring-frame and a lid. Ground vias connecting the lead-frame to the plate through the substrate may also be included. The present package is designed by modelling the various elements of the package as a coaxial transmission line, a co-planar waveguide, and a single lead in a trough transmission line in combination. In an alternative embodiment, the U-shaped via may be formed of discrete holes drilled through the substrate, rather than as a continuous U-shape.

7 Claims, 9 Drawing Sheets



Relevant

FIG. 1
PRIOR ART

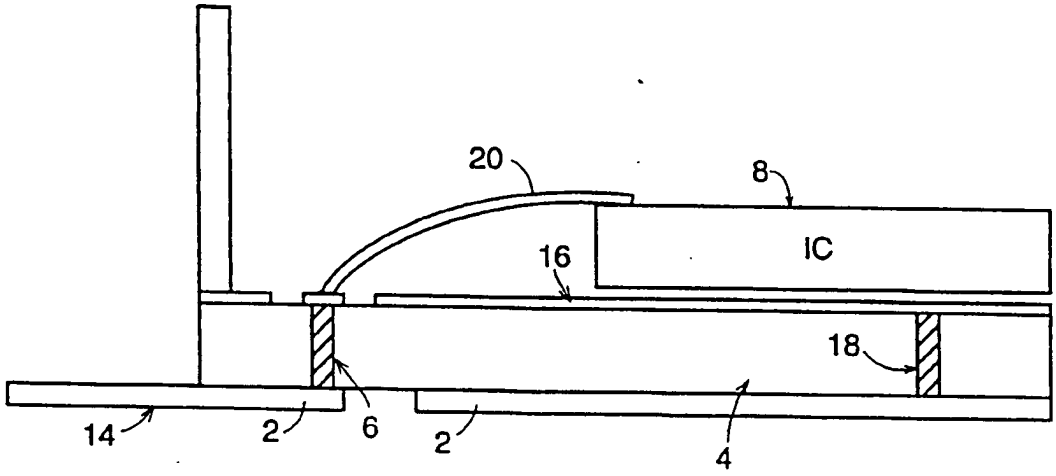


FIG. 2
PRIOR ART

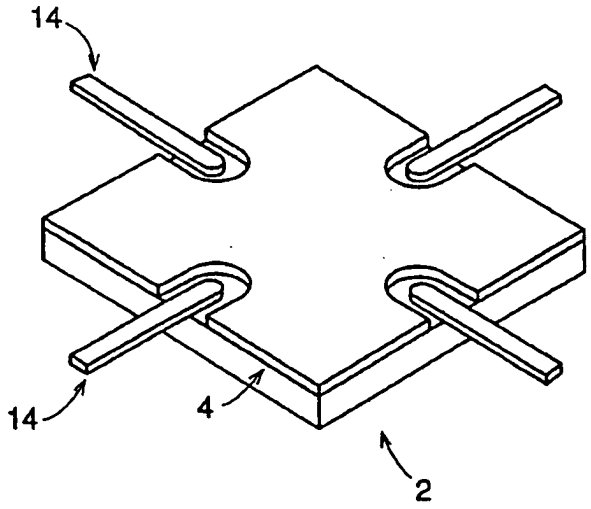


FIG. 3
PRIOR ART

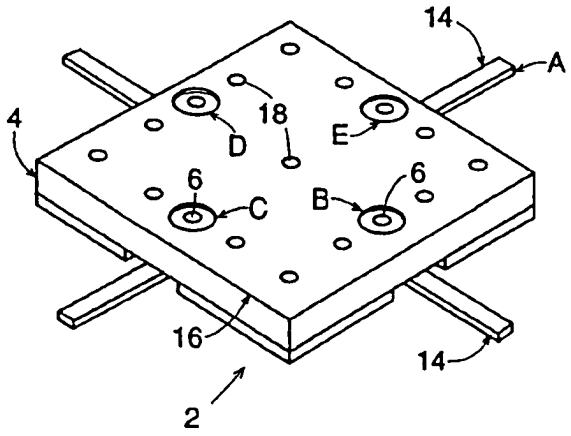
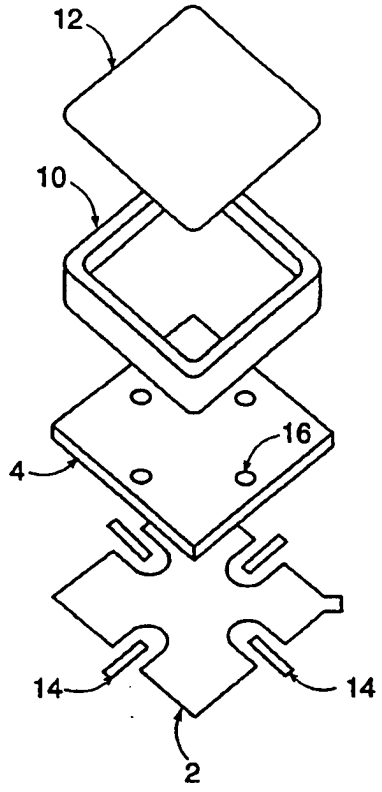


FIG. 4
PRIOR ART



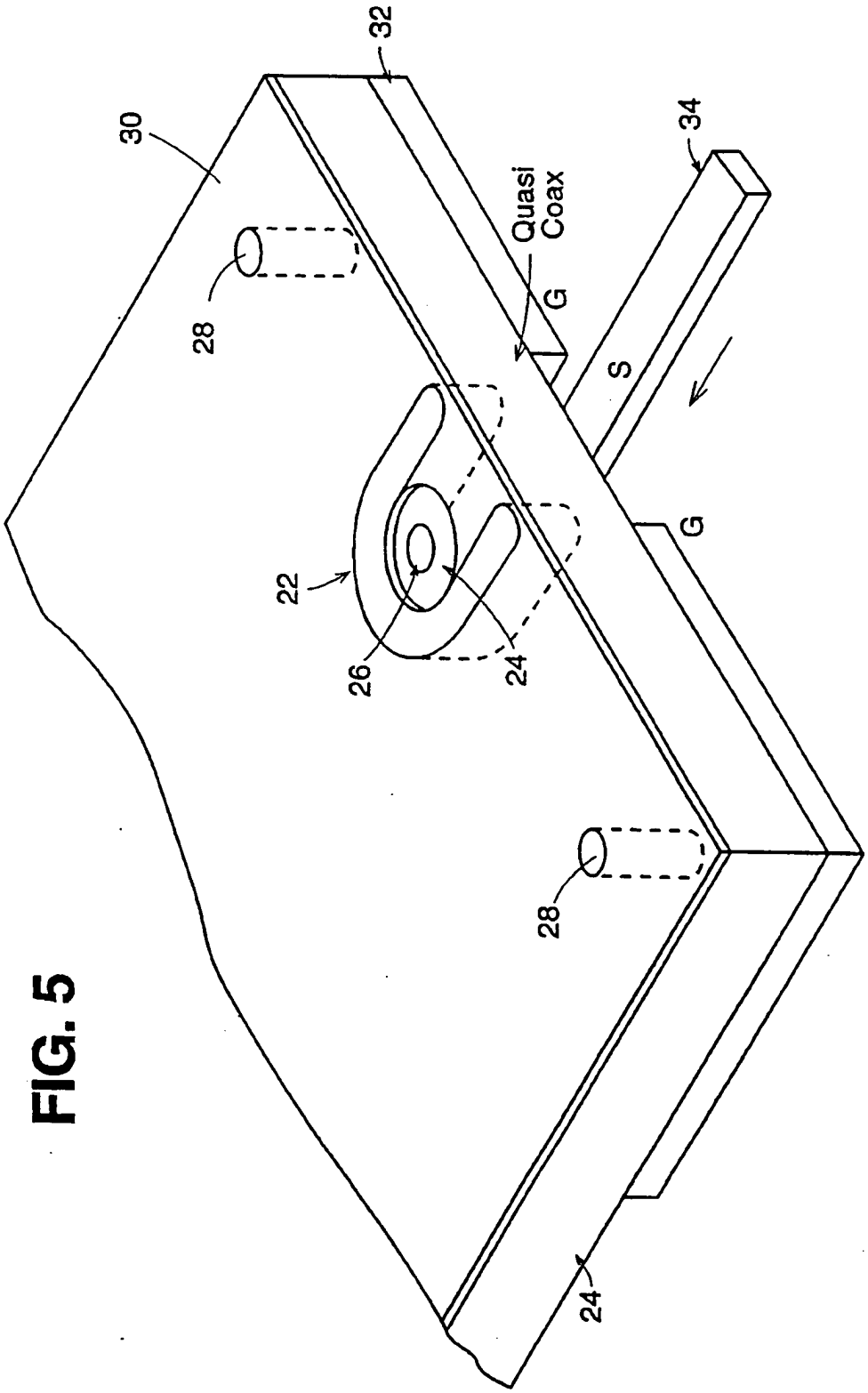


FIG. 5

FIG. 6

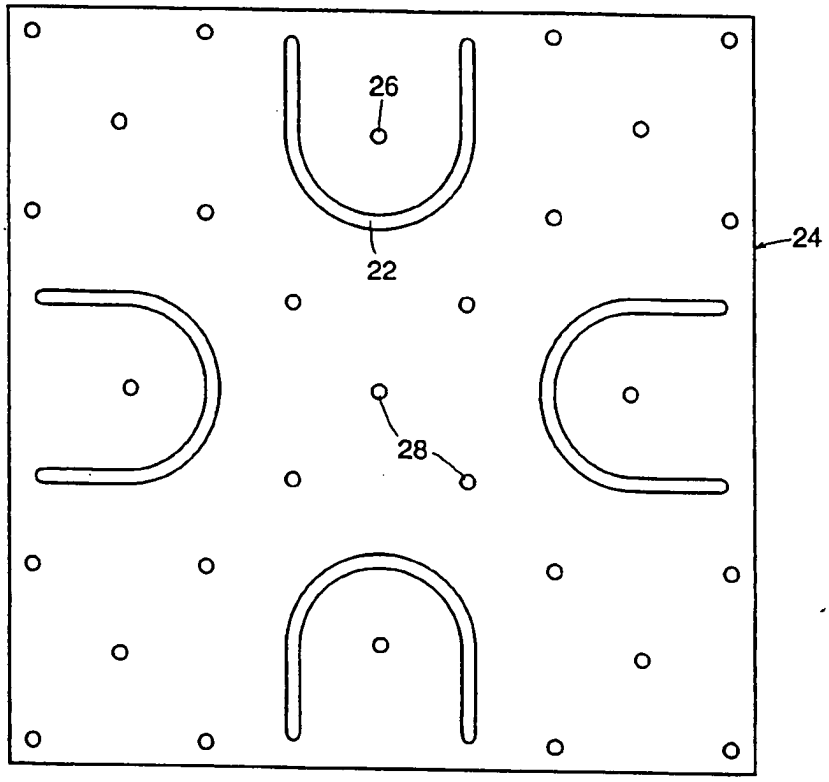


FIG. 9

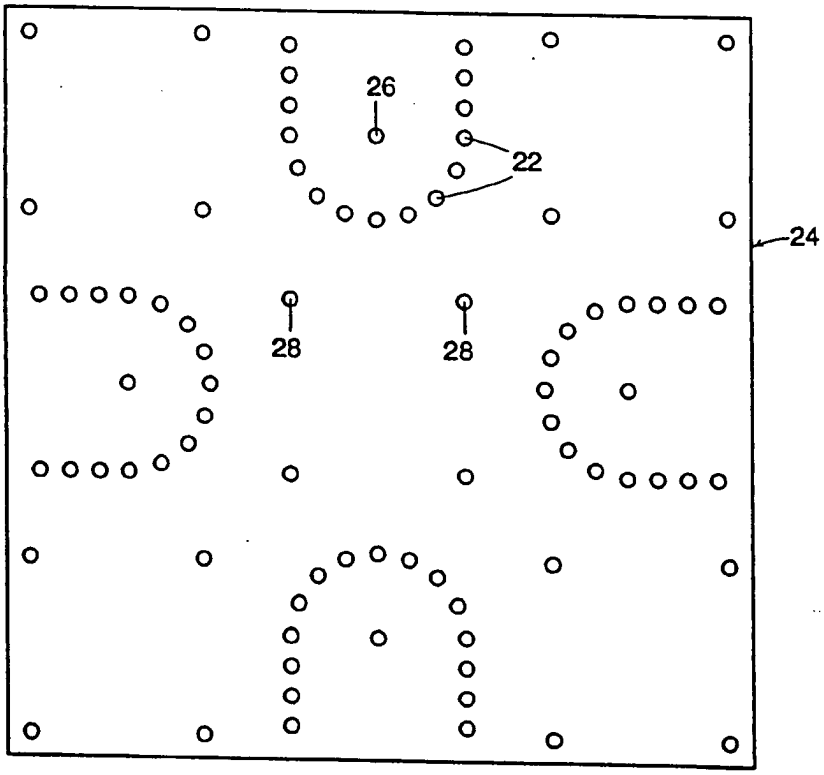


FIG. 7

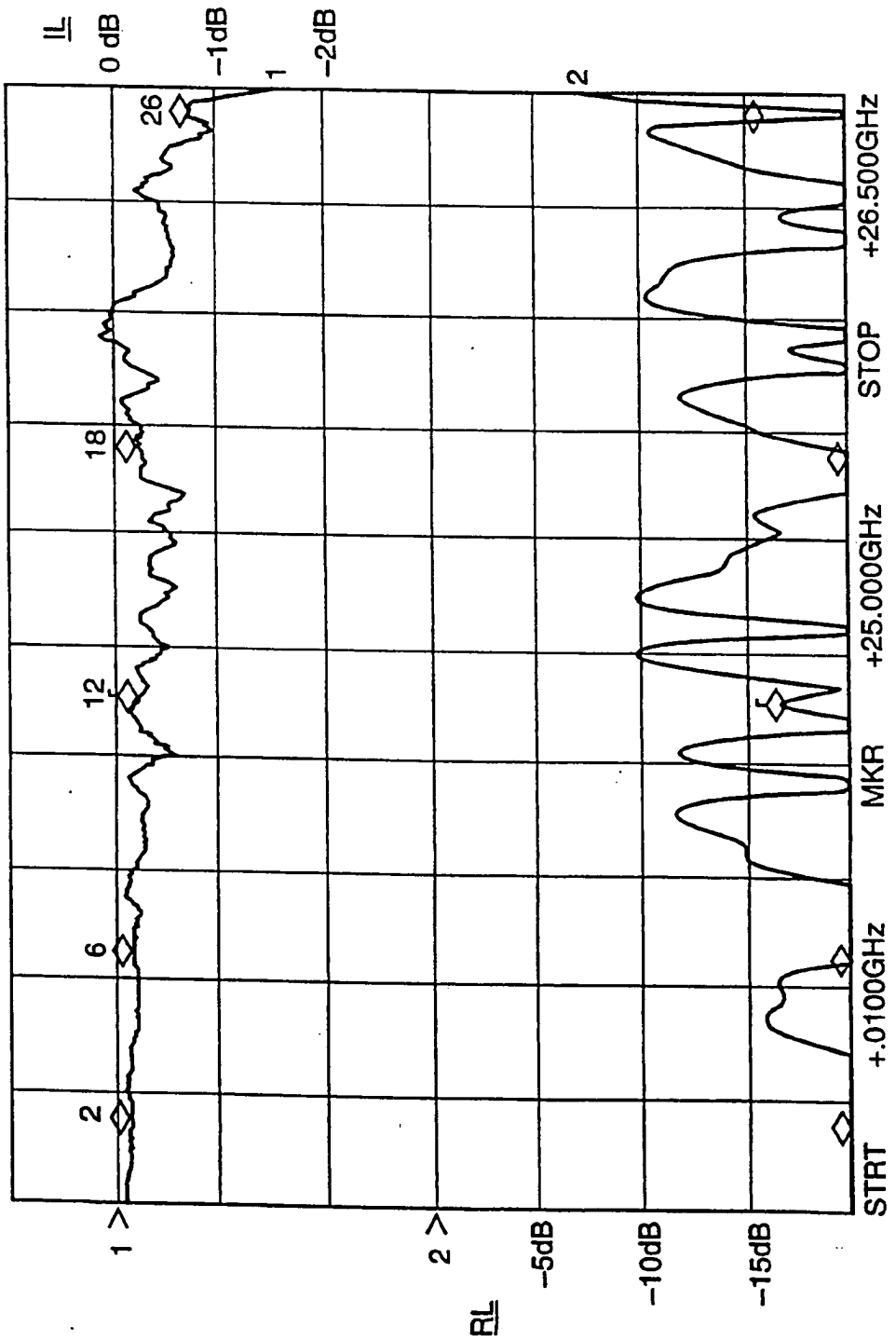

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FIG. 8

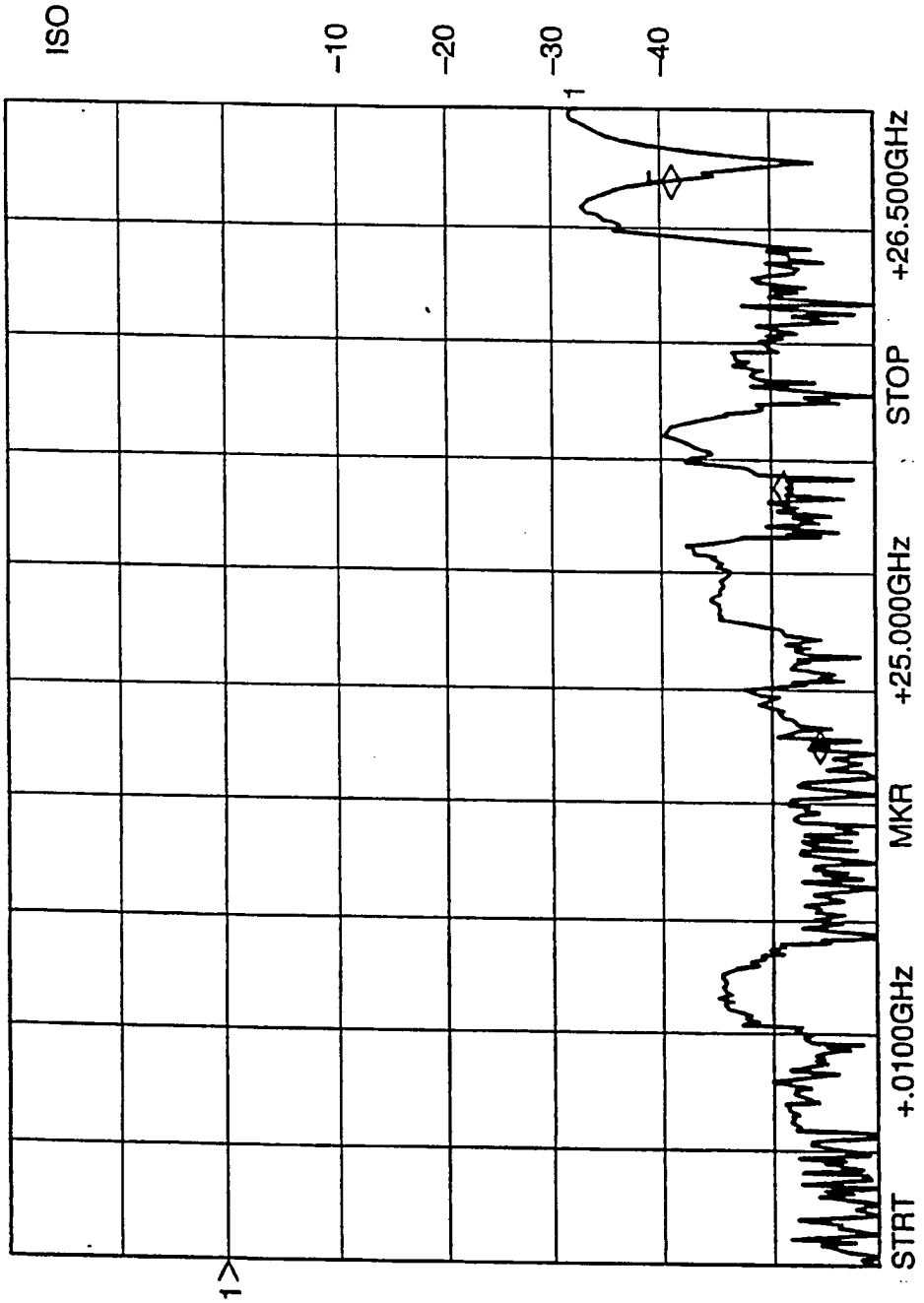

FIG. 10

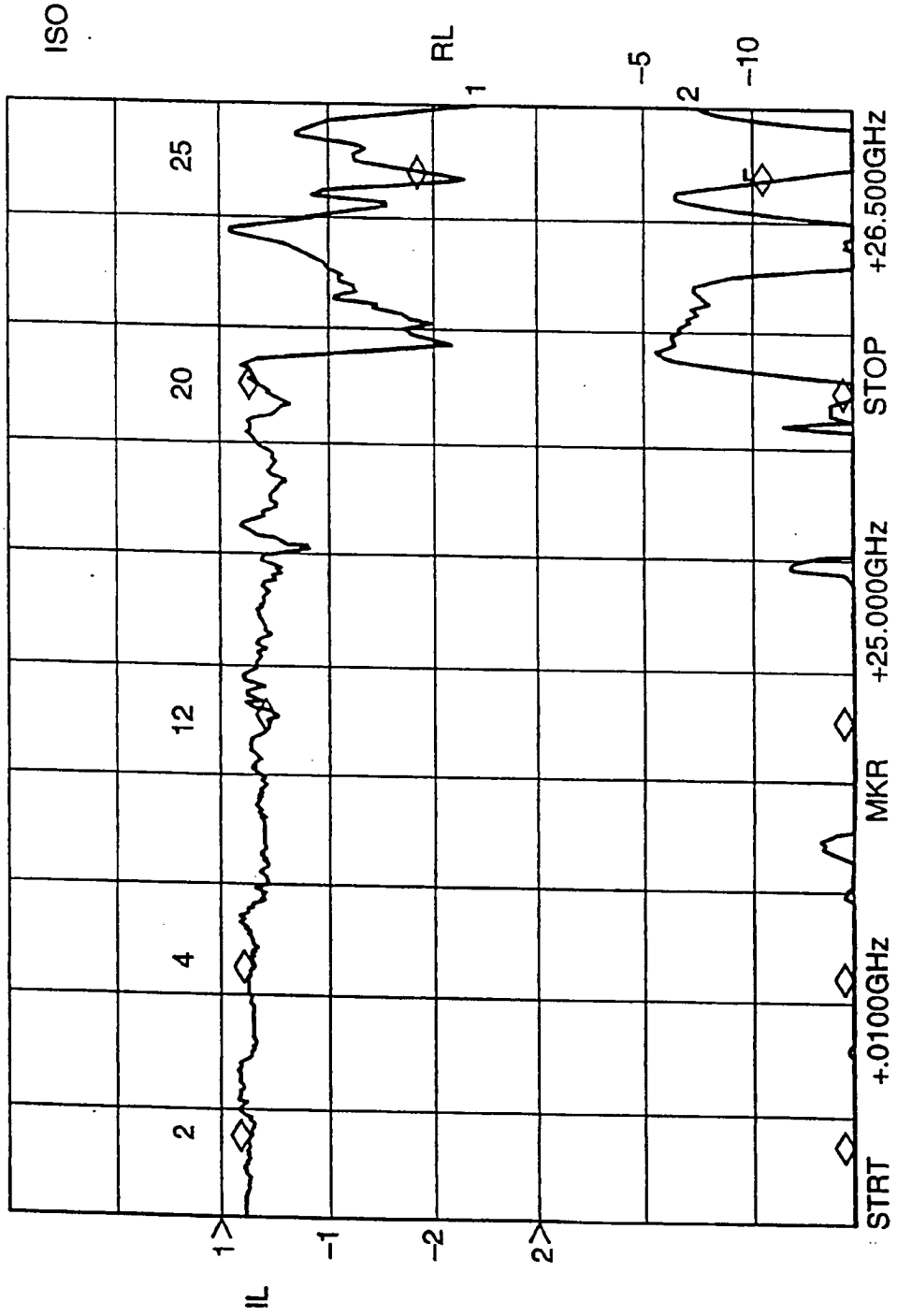
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FIG. 11

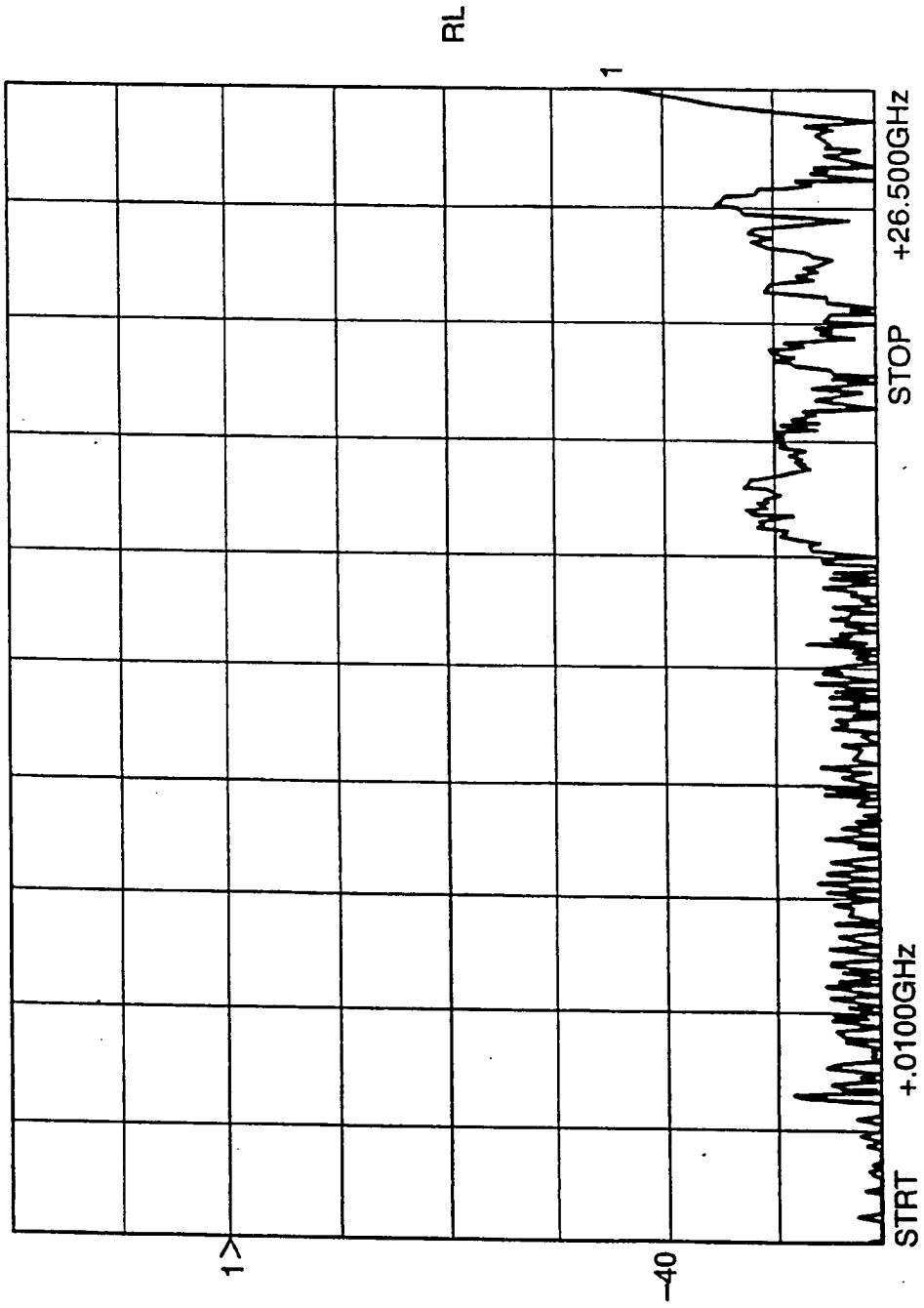
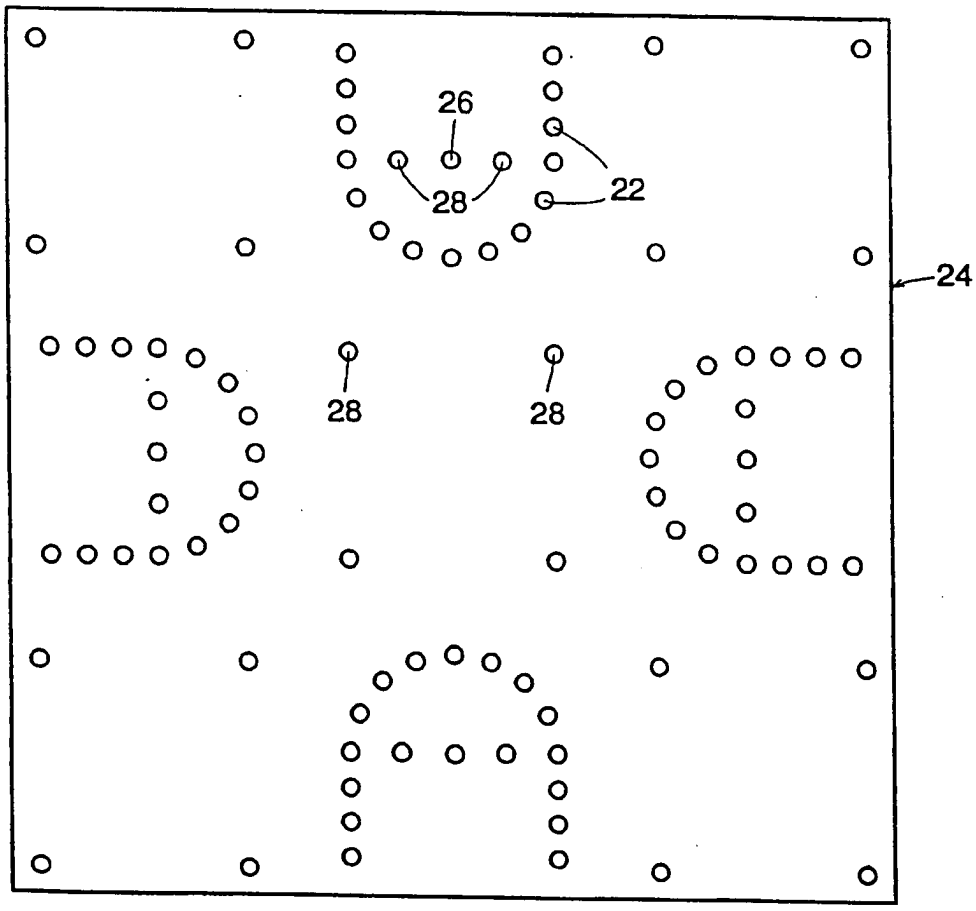


FIG. 12



MICROWAVE SURFACE MOUNT PACKAGE

This is a divisional of U.S. application Ser. No. 08/072,819, filed Jun. 7, 1993 now U.S. Pat. No. 5,401,912.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to surface mount packages for integrated circuits and more particularly to a surface mount package having a U-shaped via extending around the transmission via of the package substrate to allow the integrated circuit to be operated at higher microwave frequencies.

2. Description of the Prior Art

Surface mount packages, such as shown in Scieroe et al., U.S. Pat. No. 5,117,068, are readily known in the art. In general the purpose of such packages is to house integrated circuits in an environmentally protected enclosure, while at the same time providing electrical connections from the external package leads to the internal enclosed integrated circuit. As illustrated in FIGS. 1–4, a typical prior art surface mount package includes a lead-frame 2 which preferably matches the lead-frame of a conventional TO-8 package and includes outwardly extending leads 14 such as input, output and bias leads. A substrate 4, preferably of alumina, includes solid metal vias 6 extending therethrough which electrically connect the lead-frame 2 to an integrated circuit 8 mounted in the package. The lead-frame 2 and a seal-ring 10 are brazed to each face of the alumina base 4 in a brazing operation. After inserting the integrated circuit into the package, lid 12 is sealed to seal-ring 10 to complete the package.

The integrated circuit 8 is connected to the internal floor of the package by means of conductive epoxy or metal attach 16. Ground vias 18 are provided to electrically connect the internal ground plane 16 to the lead frame 2. Internal package leads 20, which are fabricated as part of the surface mount package make the electrical connections from the integrated circuit 8 to the lead vias 6. The metal filled vias 6 are connected to the external leads 14 during a braze operation.

As the AC frequency of the signal being sent to the IC through lead vias 6 increases beyond about 8 GHz in prior art surface mount packages, it has been found that the electrical losses and interference in the package increase beyond acceptable limits. This is so because, in microwave applications, the transmission medium and device interconnections introduce inductance and capacitance which degrade system performance. Accordingly, it is desirable to have a surface mount package suitable for frequencies beyond 8 GHz in which high frequency devices, such as cellular radio, may operate. Furthermore, it is desirable to have a method for increasing the usable frequency range of other types of integrated circuits.

SUMMARY OF THE INVENTION

The present invention is an improved system and method for reducing losses and interference in a surface mount package to make the package operable at frequencies up to 26 GHz and beyond with acceptable performance characteristics. Furthermore, the present invention is applicable for use in other types of circuits which employ a transmission lead passing through an insulating substrate.

In the present invention, the electrical impedance in the conductive elements of the surface mount package is controlled to reduce insertion loss, return loss, and to improve isolation. This is accomplished by fabricating a U-shaped via around the lead via in the surface mount package to form a quasi-coaxial transmission line through the insulating substrate. The substrate is coated on its top and bottom surfaces with a lead-frame and a plate to which an integrated circuit in the package is attached. Ground vias connecting the lead-frame to the plate through the substrate may also be provided.

To reduce losses and to improve isolation, the present package is designed using impedance matching techniques known in the art: The plate on top of the substrate and the lead via forming a coaxial transmission line; the lead frame and lead forming a co-planar waveguide; and within the substrate, the transmission via and U-shaped via forming a single lead in a trough transmission line. These elements are preferably designed to have an impedance of 50 ohms.

If desired, additional ground vias may be located in the substrate at various locations to limit ring-frame resonance effects. In an alternative embodiment, the U-shaped via may be formed by making discrete holes through the substrate in a U-shape.

Accordingly, the novel U-shaped via of the present invention provides a method whereby the usable frequency range of surface mount packages and other electrical device is increased.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a partial side view of a prior art surface mount package.

FIG. 2 shows a bottom view of a prior art surface mount package without a ring-frame.

FIG. 3 shows a top view of a prior art surface mount package without a ring-frame.

FIG. 4 shows an exploded perspective view of a prior art surface mount package.

FIG. 5 shows a partial perspective view of the surface mount package of the present invention.

FIG. 6 shows a top view of the preferred embodiment of the surface mount package substrate of the present invention.

FIG. 7 shows the insertion and return loss performance of the embodiment of the present invention shown in FIG. 6.

FIG. 8 shows the isolation performance of the embodiment of the present invention shown in FIG. 6.

FIG. 9 shows a top view of an alternative embodiment of the surface mount package of the present invention, wherein the U-shaped via is non-continuous.

FIG. 10 shows the insertion and return loss performance of the embodiment of the present invention shown in FIG. 9.

FIG. 11 shows the isolation performance of the embodiment of the present invention shown in FIG. 9.

FIG. 12 shows an alternative embodiment of the present invention wherein ground vias are located within the U-shaped via.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides an improved system and method for reducing losses and interference in a surface mount package so as to make the package operable at

frequencies up to 26 GHz and beyond. To operate at microwave frequencies, the electrical impedance in the electrical transmission lines of the present invention is controlled and the R.F. energy treated in a manner which is conducive to use at high microwave frequencies. With a typical four lead surface mount package such as shown in the prior art, three RF characteristics are important: Insertion Loss, Return Loss, and Isolation.

Insertion Loss is the amount of energy lost resulting from the transmission of RF energy. As shown in FIG. 3, this loss would be measured from the external lead to the internal connection terminal, i.e., the loss resulting from RF transmission between points A and E. The main property affecting Insertion Loss is the electrical conductivity of the metals used for transmitting the AC signal. The lowest possible loss is desired.

Return Loss is the amount of energy returning back to the terminal from which the transmitted signal originated. In FIG. 3, energy transmitted from point A to point E and reflected back to point A would constitute Return Loss. Zero reflections would be ideal, however industry standards for acceptable levels have been established. To reduce Return Loss, it is preferable to create a 50 ohm transmission line from point A to point E.

Isolation is a measure of energy leakage from one lead to another. In FIG. 3, if an R.F. signal is transmitted through the lead at point A, it is desirable that no energy be present in leads B, C, or D resulting from the energy present in lead A. These losses may be minimized by containing the electromagnetic fields throughout the package, and especially through the lead vias 6.

Prior art surface mount packages experience high RF losses at frequencies past 8 GHz. While the bottom side (see FIG. 2) of prior art surface mount packages had been designed for 50 ohms using a co-planar waveguide medium for transmission which helps to reduce losses, once the R.F. signal enters the ceramic substrate 4, losses increase beyond acceptable limits. To an extent, these losses are believed to be caused by the impedance within the lead vias 6, and by the connections between the vias 6 and the leads 14 and IC 8. The impedance within these layers and at their barriers is controlled very little if at all in the prior art. Furthermore, the via structure created within the substrate can be viewed as a waveguide without sidewalls. Within this ceramic medium, several waveguide modes can be excited by the vertical metal filled via hole, which acts as an antenna. Poor isolation and multiple resonances are also believed to occur.

As shown in FIGS. 5 and 6, by the present invention, the via hole pattern in the ceramic substrate is modified to rectify the above-identified problems and to boost the useability of the package to 26 GHz and beyond, it being understood that FIG. 5 represents a partial view of one lead of a typical four lead package. The modification consists of forming a U-shaped metal filled via 22 around the signal via 26 to form a quasi-coaxial transmission line through substrate 24.

Substrate 24 is preferably fabricated of alumina or aluminum nitride by any technique readily known to those skilled in the art, although it is readily foreseen that the substrate 24 may be made of any readily known insulator suitable for use as an insulating substrate. Transmission vias 26, ground vias 28, and U-shaped vias 22 are preferably laser drilled through the substrate 24. The dimensions of the vias will vary to reduce losses based upon the design equations described below. The vias 22, 26, and 28 are filled with a metal having a high electrical conductivity and high thermal conductivity, preferably tungsten-copper or gold. The high electrical conductivity is preferable for reducing insertion and DC losses. High thermal conductivity is preferable to provide a thermal path through the vias and out of the package which is helpful for cooling the package. It is readily foreseen that vias 22, 26 and 28 may be metal-filled with various materials and through various techniques as are known in the art.

Substrate 24 is preferably coated on its top and bottom surfaces, preferably with two layers: a first layer of titanium-tungsten is preferably sputtered on the alumina or other insulator 24 to improve adherence of the second layer, which is preferably of sputtered gold. The integrated circuit to be mounted in the package preferably sits on the upper layer of gold 30. The layer of gold on the bottom of the substrate preferably forms a conventional lead-frame 32.

The present invention may be operated at higher frequencies than prior art devices by modelling the various components of the package and then designing each element so as to minimize losses. The present invention may be modelled as three discrete elements, cooperating to reduce losses:

[1] As shown in FIG. 5, at the top of substrate 24, the transmission via 26 and ground metal 30 form a coaxial transmission line. The coaxial transmission line is formed by the lead via 26, which is the inner conductive element, and the gold plate 30 on substrate 24, which completely surrounds the lead via 26 and is the outer element of the coaxial transmission line.

The coaxial porion of the present invention is preferably designed using the following equation which is readily known in the art, where D is the diameter of the outer conductor, d is the diameter of the inner conductor, and ϵ_r is the relative dielectric constant of the dielectric between the inner and outer conductors:

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{D}{d}\right)$$

As previously indicated, the preferred characteristic Impedance Z_0 for a coaxial transmission line is 50Ω. Accordingly, the dimensions of D and d may be determined from the following equation:

$$D = de^{\left[\frac{50\sqrt{\epsilon_r}}{60}\right]}$$

[2] At the bottom of the package, where the lead 34 enters the lead frame 32 and contacts the transmission via 26, a co-planar waveguide is formed. The dimensions of the lead frame 32, the lead 34, the height of the substrate 24, and the spacing therebetween are preferably designed to minimize electrical losses and interference of a signal travelling through lead 34, and are further designed to match the impedance at the junction between lead 34 and transmission via 26. The equations for designing these elements are known in the art. These equations are complex and are preferably done using computer software specially designed for this purpose.

[3] Within the substrate, the transmission via 26 and U-shaped via 22 form a single lead in a trough transmission line. Accordingly, the dimensions of the various elements may be determined from the following equation which is known in the art, where w represents the inside width of the U-shaped via, h represents the distance between the inside lower edge of the U-shaped via 22 and the center of

transmission via 26, ϵ_r is the relative dielectric constant of the dielectric 24, Z_0 is the characteristic impedance for the transmission line which is preferably is 50Ω, d is the width of the conductive via 26, and d <<h, w.

$$Z_0 = \left(\frac{138}{\epsilon^{1/2}}\right) \log\left(\frac{4w \tanh\left(\pi \frac{h}{w}\right)}{\pi d}\right)$$

This structure is preferably designed to have an impedance of 50 ohms. Preferably, transmission via 26 is centered with respect to the width w of U-shaped via 22.

FIG. 7 shows the insertion and return loss performance of the embodiment of the present invention shown in FIG. 6. FIG. 8 shows the isolation performance of the embodiment of the present invention shown in FIG. 6.

Accordingly, by the present invention the surface mount packages is designed as three distinct electrical elements which are matched to each other so as to reduce system losses. If desired, as shown in FIGS. 5, 6 and 9, ground vias 28 may be placed in the substrate 24 at locations around the vias 26 to limit potential ring-frame resonance effects. The U-shaped via 22 controls the impedance within the ceramic and contains the electromagnetic field within a localized area, thus reducing leakage to other leads. While it has been found that utilizing a U-shaped via 22 around transmission via 26 is preferred from a manufacturing standpoint, it is foreseen that the present invention may be modified so that via 22 extends completely around transmission via 26. In this embodiment, rather than modelling the transmission via 26 thorough the substrate 24 as a "single wire in a trough," it would be modelled as a true coaxial transmission line.

FIGS. 9–11 show an alternative embodiment of the present invention, and performance characteristics up to 26.5 GHz for this embodiment. As shown in FIG. 9, U-shaped via 22 need not be continuous, but rather may be formed by a series of vias around the transmission via 26. As shown in FIG. 12, ground vias 28 may be located within the U-shaped via 22, if desired.

Although the present invention has been described with respect to utilizing U-shaped vias to reduce losses in a surface mount package, those skilled in the art would realize the applicability of the present invention to other types of electrical devices. For example, any semiconductor device having a transmission line passing through a substrate, wherein electrical interference is a problem could be modified through the addition of a U-shaped or round via around the transmission line. Furthermore, while it has been found that a U-shaped via is preferable, it is foreseen that other shaped vias around the transmission via may also provide beneficial interference and loss reduction and are within the scope of the present invention as defined in the following claims.

What is claimed is:

1. A method of fabricating a device for allowing a signal to pass through a substrate with reduced electrical losses and interference, said method comprising:

fabricating an insulating substrate having first and second opposed surfaces;

drilling a lead via hole through said insulating substrate from said first surface to said second surface;

drilling a U-shaped via through said insulating substrate from said first surface to said second surface, said U-shaped via extending at least partially circumferentially around said lead via hole;

filling said lead via hole with a conductive material, thereby forming a lead via, for allowing a lead carrying said signal to be attached to a first end of said lead via and a second lead for receiving said signal to be attached to a second end of said lead via; and

filling said U-shaped via with a conductive material.

2. The method according to claim 1 wherein the step of drilling said U-shaped via comprises drilling a plurality of separate vias in a U-shape around said lead via hole, and the step of filling said U-shaped via comprises filling each of said plurality of separate vias.

3. The method according to claim 1 further comprising the step of patterning an electrically conductive lead frame on said first surface of said substrate and grounding a portion of said lead frame, said U-shaped via being electrically connected to said grounded portion of said lead frame.

4. The method according to claim 3 further comprising the step of patterning a conductive plate on said second surface of said substrate, said plate comprising a hole extending around said lead via for enabling an electrical connection to be made to said lead via, said plate being electrically insulated from said lead via, and wherein said U-shaped via is electrically connected to said plate for grounding said plate.

5. The method according to claim 1 further comprising the step of determining the dimensions of said lead via, said U-shaped via and said substrate by modelling said device as a single wire in a trough.

6. The method according to claim 4 further comprising the step of determining the dimensions of said lead via, said U-shaped via, said lead frame, said plate and said substrate by modelling said device as a single wire in a trough, a coaxial transmission line and a quasi-coaxial transmission line.

7. The method according to claim 1 further comprising the step of drilling a ground hole from said first surface to said second surface and filling said ground hole with a conductive material.

* * * * *

US005734560A

United States Patent [19]

Kamperman et al.

[11] Patent Number: 5,734,560

[45] Date of Patent: Mar. 31, 1998

[54] **CAP PROVIDING FLAT SURFACE FOR DCA AND SOLDER BALL ATTACH AND FOR SEALING PLATED THROUGH HOLES, MULTI-LAYER ELECTRONIC STURCTURES INCLUDING THE CAP**

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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **619,096**

[22] Filed: **Mar. 20, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 352,144, Dec. 1, 1994, abandoned.

[51] Int. Cl.[6] **H01R 9/00**

[52] U.S. Cl. 361/774; 174/255; 174/262; 174/261; 257/738; 361/777; 361/792

[58] Field of Search 174/250, 255, 174/261, 262–266; 228/180.21, 180.22; 257/700, 723, 724, 737, 738, 778; 361/760, 767, 768, 771, 772, 773, 774, 777, 779, 780, 782, 783, 792–794, 795, 803; 439/68, 69, 83, 47, 74, 85

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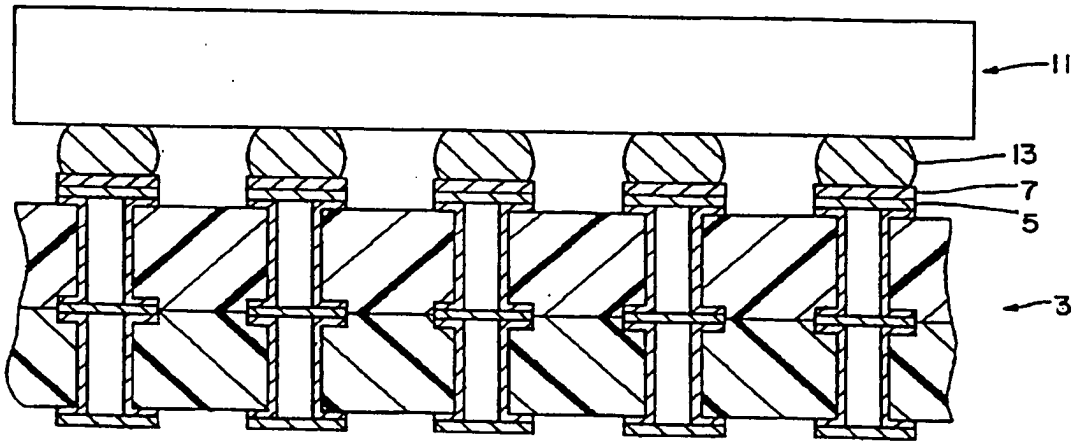
Primary Examiner—Donald Sparks

Attorney, Agent, or Firm—Pollock, Vande Sande & Priddy

[57] **ABSTRACT**

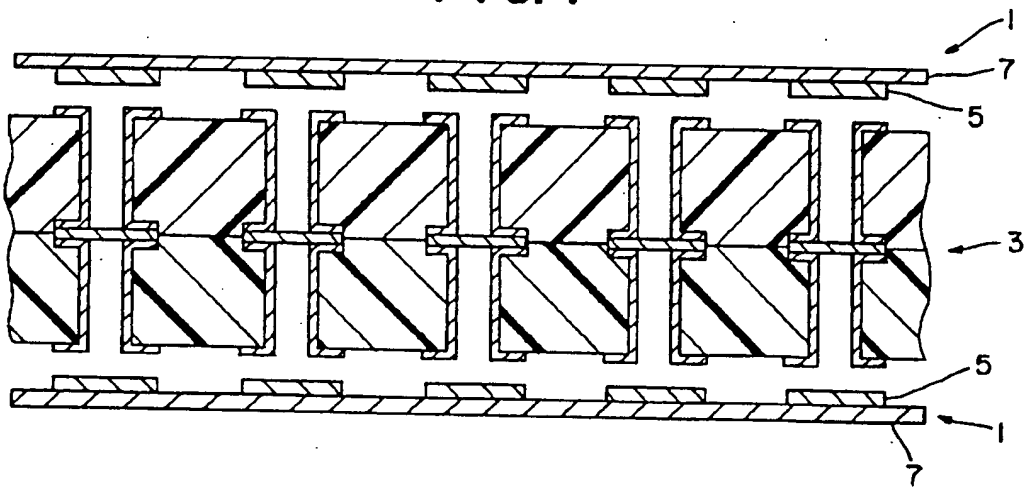
A cap for attaching a chip or other device to a multi-layer electronic structure. The cap includes a plurality of pads of an electrically-conducting material attached over plated through holes of the multi-layer electronic structure. Each of the pads includes a flat upper surface for attaching the chip or other device to the multi-layer structure, provides an electrical connection between the chip or other device and the multi-layer structure, and seals the through holes to prevent solder from entering the plated through hole. The pads are physically isolated from each other.

14 Claims, 1 Drawing Sheet



Not - Relevant

FIG. 1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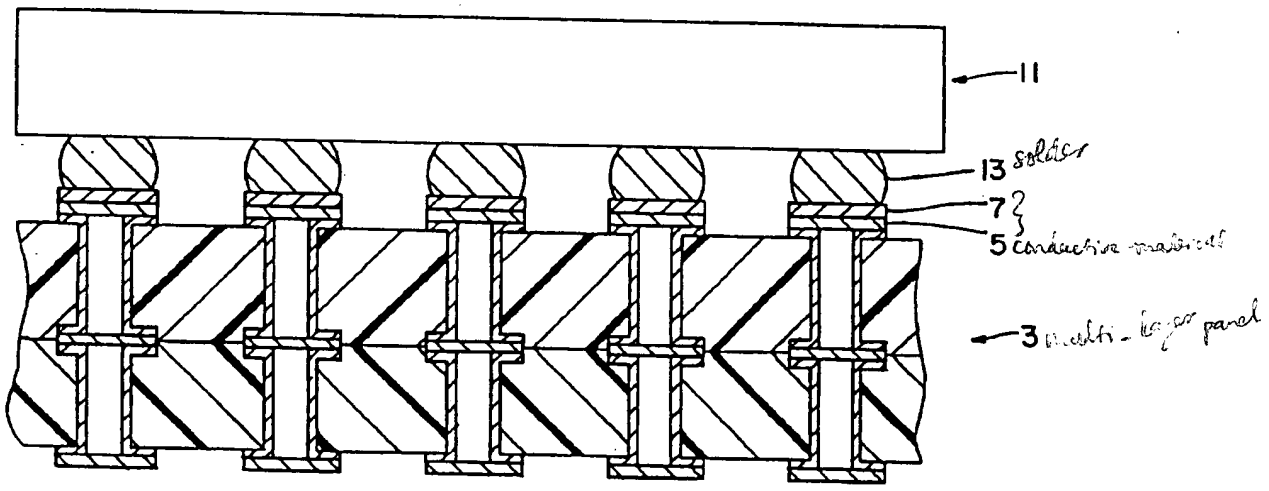
11
13 solder
7
5 conductive material
3 multi-layer panel

FIG. 2

CAP PROVIDING FLAT SURFACE FOR DCA AND SOLDER BALL ATTACH AND FOR SEALING PLATED THROUGH HOLES, MULTI-LAYER ELECTRONIC STURCTURES INCLUDING THE CAP

This application is a Continuation of U.S. patent application Ser. No. 08/352,144, filed Dec. 1, 1994 now abandoned.

FIELD OF THE INVENTION

The present invention relates to a structure for attaching devices to multi-layer electronic structures, such as circuit boards and cards. The invention also relates to methods for forming multi-layer electronic structures and to attaching electronic devices, such as integrated semi-conductor chips to multi-layer electronic structures.

BACKGROUND OF THE INVENTION

Multi-layer electronic structures such as circuit boards, circuit cards, chip carriers and other such devices typically are formed from a plurality of electrically conducting and electrically insulating planes. The electrically conducting planes function as ground, signal, and/or power planes and conduct electrical current from an attached electrical device to what ever the multi-layer structure is electrically connected to.

Usually, multi-layer electronic structures include a plurality of mounting sites on one or both surfaces to which a semiconductor chip or other electronic device is attached. Typically, the sites are made of an electrically conducting material and function as ground, power, and/or signal sites. Usually, the pattern of attachment sites on the structure, matches a pattern of power, ground, or signals sites on the attached device. The power, ground and/or signal connecting sites between the multi-layer structure and the chip or other attached device preferably are connected to the plurality of plated through holes formed through the multi-layer structure.

In forming the multi-layer circuit board or card, a plurality of printed circuit cores may first be formed and then joined to form the multi-layer structure. In such a procedure, each core typically is constructed from at least one plane of at least one electrically conducting material surrounded on both sides by a plane of at least one electrically insulating material. A plurality of through holes may then be formed in the electrically insulating and electrically conducting planes. Next, an electrically conducting material may be plated on the surface of the through holes.

In another embodiment, the cores are formed as described above. A plurality of holes are formed through the outer electrically insulating planes but not through the electrically conducting plane. These holes are then filled with an electrically conducting material. Such filled holes are commonly known as mounting or joining studs.

When using either of these methods to form the cores, a plurality of the cores are then stacked on top of each other and aligned so that the plated through holes or joining studs on adjacent cores are aligned. The stack of cores is then subjected to elevated temperatures and pressures so as to cause the electrically insulating material and the electrically conducting material on facing surfaces of adjacent cores or adjoining studs on adjacent cores to be joined together.

The composite multi-layer panel may also be processed by forming contacts for electrically connecting a chip or other device to the panel. Such contact sites may be formed by drilling a plurality of holes in the top surface of the panel and then depositing an electrically conductive material in the holes, similarly to the method described above used for providing mounting between cores of the composite. The filled holes may be electrically connected to the electrically conducting planes of the composite. The ground, signal, and power sites on a chip or other device are then aligned with the sites on the panel and then bonded thereto.

However, as device dimensions have decreased, and the number of mounting sites on chips and circuit boards has increased, the spacing between mounting sites has decreased. This makes it more difficult to join the chips and other devices to multi-layer composites and still provide a solder dam or other means for preventing solder from flowing away from the mounting sites.

SUMMARY OF THE INVENTION

The inventors of the present invention recognized the above-discussed problems, among others, and developed the present invention to over come these problems and other short comings of the prior art.

An object of the present invention is to provide a cap structure for attaching to a multi-layer composite electronic structure for providing an improved surface for mounting electronic devices.

An advantage of the present invention is to improve the multi-layer surface for attaching electronic devices to a multi-layer electronic composite enabling greater interconnect density.

In accordance with preferred aspects, the present invention provides a process of forming a multi-layer electronic composite structure. The process includes the step of providing at least one core including at least one plane of at least one electrically conducting material with a plane of at least one electrically insulating material on both sides of the at least one plane of at least one electrically conducting material. The at least one core also includes a plurality of plated through holes formed therethrough. Also according to the process, a pad is provided over at least one of the plated through holes. The pad provides a flat surface for attaching an electronic device and also prevents solder from entering the at least one plated through hole.

According to other preferred aspects, the present invention provides a cap for attaching a chip or other device to a surface of a multi-layer electronic structure. The multi-layer electronic structure includes a plurality of plated through holes formed through it. The cap includes a pad attached over at least one of the plated through holes of the multi-layer electronic structure. The pad includes a flat upper surface for attaching the chip or other device to the multi-layer structure and for sealing the plated through hole to prevent solder from entering the through hole.

According to further preferred aspects, the present invention provides a multi-layer electronic structure including at least one core including at least one plane of at least one electrically conducting material having a plane of at least one electrically insulating material on both sides of the at least one plane of at least one electrically conducting material. The at least one core includes a plurality of plated through holes formed therethrough. The multi-layer electronic structure also includes a pad attached over at least one of the plated through holes.

Still other objects and advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description, wherein it is shown and

described only the preferred embodiments of the invention, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 represents a cross sectional view of a portion of a multi-layer circuit panel according to the present invention and top and bottom cap layers according to the present invention prior to attachment to the multi-layer panel; and

FIG. 2 represents a cross sectional view of an electronic device attached to an embodiment of a cap structure of the present invention, with the cap structure attached to a multi-layer circuit panel.

DETAILED DESCRIPTION OF VARIOUS AND PREFERRED EMBODIMENTS

As stated above, as the dimensions of circuits on chips have been reduced, the number of circuits on a chip has increased and the number of electrical connections which must be made to the chip has increased. The density of the ground, power, and signal sites on the chip to be attached to a circuit board or card or chip carrier have also increased. This increased number of attachment sites creates a number of problems, among them being the available space on the surface of the circuit board or card for assembly pads and plated holes.

Commonly known methods for directly attaching chips to another structure, such as a circuit board or card, require pads for attaching the chip. With an increased number of devices on chips and an increased number of input and output sites on chips, direct chip attach methods require pads on a fine area array pitch. For instance, the pitch may be on the order of about 8 to about 10 mil center-to-center spacing between pads.

According to known methods, if the holes used in forming the attachment sites in the circuit board or card are drilled, pads approximately 5 mil in diameter around holes about 3 mil in diameter are the smallest dimensions currently practical in commercial, mass-produced printed circuit board technology. Frequently, the pads are offset from the drilled holes and are provided with a solder dam to prevent the solder from wicking down the holes. However, as can be seen from the dimensions of the holes, pads, and array, the 9 mil grid of 5 mil pads leaves very little space for offsetting the pads from the drilled holes. Additionally, with this spacing little room remains for providing a solder dam between the plated through hole and bonding pad.

Mounting chips or solder balls, typically used in mounting chips or other devices, on drilled holes requires a method for plugging the holes to prevent solder from wicking away from the joint. Arranging the mounting pads directly over the drilled holes provides a maximum density of input and output sites and eliminates the need for a solder mask. However, this technique requires a flat surface.

One solution to the above problems has been to fill vias in the circuit board with solder. However, typical solders cannot withstand high temperatures associated with many processing steps used in processing circuit boards. Additionally, when depositing solder in holes in a circuit board, it is very difficult, if not impossible, to obtain a flat surface since the exact amount of solder cannot be easily known.

To provide an improved method and structure for attaching chips and other devices to circuit boards and cards, the present invention provides a method and structure for a multi-layer composite panel with a top surface including electrical conductors for attaching devices built in a separate parallel process and then joined to the multi-layer composite in a lamination process. The resulting structure preferably provides a flat surface suitable for direct chip attach. By providing a cap on the top and/or bottom surface of the multi-layer circuit board, the present invention provides top and/or bottom surfaces of the multi-layer composite which are flat and facilitate the plating of solder. The surface of the cap may be patterned so as to leave discrete conductors surrounded by dielectric material thereby eliminating the need for a solder mask to be added to the panel.

The capping process of the present invention also allows electroplating solder for attaching devices, eliminating the need for sputtering or plating an electrical commoning layer on the composite circuit. Additionally, the present invention provides a method of building such a cap. Further, the present invention is a method for providing a solder layer on a multi-layer circuit board composite by depositing solder on a carrier sheet attached to a cover sheet of an electrically conducting material. The resulting structure is laminated onto the composite circuit board.

The present invention also provides a process for forming a solder layer for a multi-layer composite, the solder layer sealing hollow vias formed in the multi-layer composite. The openings of the hollow are exposed on the top and bottom layers of the composite. By sealing these exposed open hollow vias, the cap layer of the present invention prevents materials used in processing steps subsequent to the attachment of the cap from entering the vias and becoming trapped where they may cause reliability problems.

To provide a flat surface for chip attachment, eliminate the need for a solder dam, as well as to provide other functions, the present invention provides a cap layer. The cap layer may be attached to the top and bottom layers of a circuit board or card, as needed. Further, once attached to a circuit board or card, the cap structure of the present invention may act as a hermetic seal, sealing hollow vias in the circuit board, thereby helping to prevent process chemicals employed in the solder plating and/or etch steps, among others, from entering the vias. This sealing function helps to prevent the risk of reliability due to solution trapped in the vias.

Accordingly, the present invention provides an improved structure and method of forming a structure for joining integrated semiconductor chips or other devices to a high density circuit card. According to the present invention, a cap structure may be formed separately from the multi-layer composite, such as a circuit board. The cap structure may then be attached to the top and/or bottom of the multi-layer composite. The cap structure preferably provides a flat surface for directly attaching a chip using direct chip attach methods, or alternatively solderable attachment processes including Ball Grid Array (BGA) or any other suitable attaching method. By providing a flat surface, the present invention also eliminates the need for a solder dam.

The cap structure preferably comprises a plurality of pads attached to the exposed openings of plated through holes of a circuit board or card. The pads may be attached to any number of the plated through holes. The pads preferably substantially completely seal the openings of the plated through holes. Accordingly, the pads preferably are large enough to seal the plated through holes. The exact size may vary, depending upon the application.

The pads may be formed of copper, gold, gold/tin, tin/lead, and/or any combination of these materials and/or any other electrically conducting material, alone or in combination with one or more of the above materials or in combination with another material.

Methods for forming multi-layer electronic composite structures according to the present invention include providing at least one core structure. The core structure preferably includes a plane of an electrically conducting material. A plane of an electrically insulating material may be provided on both sides of the plane of electrically conducting material. The core includes a plurality of plated through holes formed therethrough. The core may be formed according to known methods.

A pad is provided over an opening of each of the plated through holes in the at least one core. Each of the pads provides a flat surface for attaching a ground, signal, or power site of an electronic device, such as a semiconductor chip, to the pad. Each of the pads also helps to prevent solder from entering the plated through holes, thereby helping to prevent electrical and other problems associated with solder flow into the plated through holes.

Further according to methods of the present invention, a multi-layer electronic composite structure may be formed by first providing a composite panel. The composite structure may be formed from a plurality of cores, each core including at least one plane of an electrically conductive material surrounded by at least one plane of an electrically insulating material on opposite sides. A cap structure formed as described below may then be attached to the stack of cores and a device attached to the cap structure.

Forming a cap structure, according to methods of the present invention, for attaching a chip or other device to a multi-layer composite, such as a circuit board or card, may include providing a plane of an electrically conducting material. The electrically conducting material may, for instance, be copper. The copper may be in the form of a foil. The foil may be 2 ounce copper foil. However, other electrically conducting materials may be used and in different amounts.

A plurality of electrically conducting sites may be provided on one side of the plane of an electrically conducting material. The pattern of electrically connecting sites on the lower surface of the cap preferably matches the plated through hole or mounting or joining stud grid on the multi-layer composite. On the upper surface of the cap, the pattern of electrically conducting sites preferably matches the pattern of ground, signal and power sites on a chip or device to be attached to the cap and ultimately to the multi-layer composite.

The cap may then be joined to the composite circuit board on either side or on both sides of the circuit board or card. The material between the electrically conducting sites may then be removed according to known methods, thereby leaving a plurality of pads attached to each plated through hole. Then, a chip or other device may be attached to the resulting structure.

FIG. 1 shows a cross-sectional view of a portion of a multi-layer circuit panel according to the present invention and top and bottom cap 1 according to the present invention prior to attachment to the multi-layer panel 3. In FIG. 1, the electrically conducting material 5 are attached to the panel of an electrically conducting material 7. The electrically conducting material 5 forming part of the individual pads are positioned over the plated through holes 9. As described, the caps are then attached to the multi-layer structure 3.

FIG. 2 represents a cross-sectional view of an electronic device 11 attached to an embodiment of a cap of the present invention, with the cap attached to a multi-layer circuit panel. The device 11 is attached using solder balls 13. In the embodiment shown in FIG. 2, the cap comprises a plurality of pads. Each pad shown in FIG. 2 comprises the electrically conducting material 5 and the portion of the panel 7 located above the material 5. The pads have also been attached to the side of the multi-layer structure opposite the side that the device is attached to. In some embodiments, the pads may also include a further portion of electrically conducting material attached to the portion of the panel opposite the electrically conducting material 5. Although in FIG. 2, a pad is attached over each plated through hole, according to the invention, a pad may not be placed over every through hole.

The cap structures discussed above may be formed of the same material as the multi-layer composite, thereby reducing problems associated with differences in coefficients of thermal expansion. A cap structure according to the present invention may be formed by providing a carrier sheet of an electrically conducting material. The electrically conducting material may be any known electrically conducting material. For example, the electrically conducting material in the panel from which the cap structure is formed and/or the electrically conducting material plated on the panel in the pattern of the ground, power, and/or signal sites of the may be metal such as copper or copper/INVAR/copper, or any other suitable electrically conducting material.

Further embodiments of methods of the present invention of forming a multi-layer electronic composite may include the step of providing at least one core including a plane of an electrically insulating material having a plane of an electrically insulating material on both sides of the plane of electrically conducting material. The at least one core may include a plurality of plated through holes formed therethrough.

A cap may be formed by providing a panel of a plane of an electrically conducting material including a top surface and a bottom surface. A layer of a photosensitive material may be deposited on the top and bottom surface of the electrically conductive plane of the panel. Marks for aligning the cores and the cap may be provided on the cap and/or the cores. The photosensitive material on the bottom surface of the electrically conducting plane may be exposed to radiation providing sufficient energy to cause photochemical reactions to occur within the photosensitive material. The bottom surface of the cap may be exposed in a pattern matching a pattern of plated through holes formed in the at least one core. All of the photosensitive material on the top surface of the electrically conducting plane of the panel may be exposed to radiation.

The portions of the photosensitive material not exposed to the radiation may be removed. The portions of the electrically conductive layer exposed by removing the portions of the photosensitive material may be cleaned. An electrically conducting material may be deposited on the exposed portions of the electrically conducting material. The electrically conducting material may be any commonly used material. For instance, gold, gold/tin, or lead/tin solder may be used. All remaining portions of the photosensitive material from the electrically conducting plane may be removed.

The electrically conducting material deposited on the electrically conducting plane may be aligned with the plated through holes on the core. The alignment of the electrically conducting material on the electrically conductive plane with the plated through holes may be verified. The panel

may be joined to the at least one core by laminating the bottom surface of the panel to the core.

The top surface of the panel may then be cleaned and a layer of a photosensitive material deposited on the top surface of the panel. Selected portions the photosensitive material on the top surface of the panel may then be exposed to radiation. The radiation preferably causes photochemical reactions to occur within the photosensitive material. The photosensitive material may then be developed to remove portions of the photosensitive material, leaving portions either exposed or not exposed, depending upon the type of photosensitive material used.

An electrically conducting material may then be deposited on the portions of the surface of the top of the panel uncovered by the removal of the photosensitive material. The electrically conducting material forming the base of the panel may then be etched, using the just applied electrically conducting material as a mask. One etchant that may be used is ammonium chloride and cupric chloride or an equivalent etchant. Preferably, the etchant will etch the electrically conducting base material and not the just applied electrically conducting material.

In an alternative embodiment, the portions of the photosensitive material deposited on the upper surface of the panel that are not removed during development may be used as a etch mask. In such an embodiment, the panel is etched so as to remove the portions exposed by the removal of the photosensitive material. The remaining photosensitive material preferably protects the portions of the panel over the plated through holes. After etching the panel, the remaining photosensitive material may then be removed.

In an embodiment in which the remaining photosensitive material does not serve as a mask, after etching, the electrically conducting material applied where the photosensitive material was removed may be subjected to elevated temperatures to cause any organic plating additives to outgas before attempting to attach a chip or other device. The applied electrically conducting material may then be subjected to pressure to flatten or dimple the material. If the photosensitive material is used as an etch mask, then the outgassing step may be deleted and the exposed portion of the panel may be subjected to pressure to flatten or dimple the panel material. In either embodiment, prior to flattening, the pad material may heated to a temperature sufficient to reflow the material.

A device, such as a semiconductor chip, may be attached to the multi-layer structure at any point after the removal of the material between the pads, whether reflow or mechanical flattening have taken place.

The top layer of the cap structure described above could by formed from a carrier sheet made of an electrically conducting material. For example, the carrier sheet could be made of a metal. Examples of metals include copper and copper/INVAR/copper The sheet may be made from the same material as the electrically conducting plane in the cores of the circuit board. By forming the top layer of the cap from the same electrically conducting material as is used in the cores of the circuit board, problems associated with thermal expansion may be reduced or eliminated.

Advantages of the present invention include providing a flat surface to facilitate plating of solder to join a chip or other device to a multi-layer structure. The flat surface includes discreet conductors surrounded by dielectric material so that a solder mask to prevent undesirable flow of the solder is not required. Furthermore, the present invention allows for the attaching of devices without the need for sputtering or plating an electrical commoning layer on the composite panel.

A multi-layer electronic structure according to the present invention, one embodiment of which is shown in cross-section in FIG. 2, may include at least one core including a plane of an electrically conducting material with a plane of an electrically insulating material on both sides of the plane of electrically conducting material. The at least one core includes a plurality of plated through holes formed therethrough. A pad or cap is attached over at least one of the plated through holes. The pads/caps substantially completely seal the openings of the plated through holes. An electronic device including a plurality of ground, signal, and power sites, is attached to the pads/caps. Each of the ground, power, and/or signal sites is attached to one of the pads/caps. If the electronic device is attached to the pads/caps using solder balls, then the composite includes solder balls between the pads/caps and the attached electronic device.

In this disclosure, there is shown and described only the preferred embodiments of the invention, but, as aforementioned it is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.

What is claimed is:

1. A cap for attaching a chip or other device to a multi-layer electronic structure, said cap comprising:

a plurality of pads of an electrically-conducting material attached over plated through holes of the multi-layer electronic structure, each of said pads including a flat upper surface for attaching said chip or other device to said multi-layer structure, providing an electrical connection between said chip or other device and said multi-layer structure, and sealing said plated through holes to prevent solder from entering said plated through holes, said pads being physically isolated from each other.

2. A cap according to claim 1, wherein the cap comprises substantially similar electrically-conducting materials included in said multi-layer electronic structure that the cap is attached to.

3. A cap according to claim 1, wherein the electrically-conducting material of said pads is substantially similar to an electrically-conducting material of said plated through holes.

4. A cap according to claim 1, wherein the electrically-conducting material of said pads is substantially similar to an electrically-conducting material of an electrically-conducting layer of said multi-layer structure.

5. A cap according to claim 1, wherein each of said pads comprises a plurality of layers.

6. A cap according to claim 1, wherein one of said pads is attached over each of said plated through holes of said multi-layer electronic structure.

7. A multi-layer electronic structure, comprising: at least one core including a plurality of functional planes, said at least one core including a plurality of plated through holes formed therethrough; and

a plurality of pads of an electrically-conducting material attached to plated through holes of the core, each of said pads including a flat upper surface for attaching said chip or other device to said multi-layer structure, providing an electrical connection between said chip or other device and said multi-layer structure, and sealing said plated through holes to prevent solder from entering said plated through holes, said pads being physically isolated from each other.

8. A multi-layer electronic composite structure according to claim 7, further comprising:

an electronic device including a plurality of ground, signal, and power sites, at least one of said sites being attached to one of said plurality of pads.

9. A multi-layer electronic composite structure according to claim 8, wherein said electronic device is attached to said one of said pads using solder balls.

10. A multi-layer electronic composite structure according to claim 8, wherein said electronic device is directly attached to said one of said pads.

11. A multi-layer electronic structure according to claim 7, wherein the electrically-conducting material of said pads is substantially similar to an electrically-conducting material of said plated through holes.

12. A multi-layer electronic structure according to claim 7, wherein the electrically-conducting material of said pads is substantially similar to an electrically-conducting material of an electrically-conducting layer of said multi-layer structure.

13. A multi-layer electronic structure according to claim 7, wherein each of said pads comprises a plurality of layers.

14. A multi-layer structure according to claim 7, wherein one of said pads is attached over each of said plated through holes of said at least one core.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,734,560

DATED : 03/31/98

INVENTOR(S) : J. S. Kamperman et al

It is certified that error appears in the above-Indentified patent and that said Letters Patent is hereby corrected as shown below:

Title page, Item [54] and col.1, line 4,

In the Title: change "Sturctures" to "Structures"

Claim 7, line 1 after ":" start a new paragraph

Signed and Sealed this

Eleventh Day of August 1998

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

US005347086A

United States Patent [19]

Potter et al.

[11] Patent Number: 5,347,086

[45] Date of Patent: Sep. 13, 1994

[54] COAXIAL DIE AND SUBSTRATE BUMPS

[75] Inventors: Curtis N. Potter; David A. Gibson, both of Austin, Tex.; Uttam S. Ghoshal, Richmond, Calif.

[73] Assignee: Microelectronics and Computer Technology Corporation, Austin, Tex.

[21] Appl. No.: 856,501

[22] Filed: Mar. 24, 1992

[51] Int. Cl.[5] A05K 1/00

[52] U.S. Cl. ..... 174/261; 174/35 R; 174/260; 228/180.1

[58] Field of Search ..... 174/32, 35 R, 257, 261, 174/260; 228/180.1; 333/18

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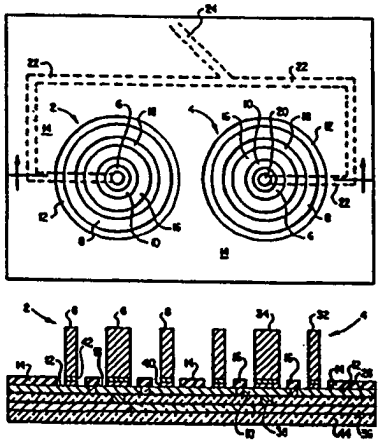
Primary Examiner—Leo P. Picard
Assistant Examiner—Cheryl R. Figlin
Attorney, Agent, or Firm—Johnson & Gibbs

[57] ABSTRACT

A coaxial bump for connecting a die to a substrate includes a center post and a ground ring surrounding and shielding the center post. The center post may be a center conductor line, and the ground ring may be generally torus-shaped, nearly closed or completely closed. The coaxial bump provides very low crosstalk in chip-to-substrate interconnections and provides a constant impedance with negligible inductive discontinuity.

18 Claims, 2 Drawing Sheets



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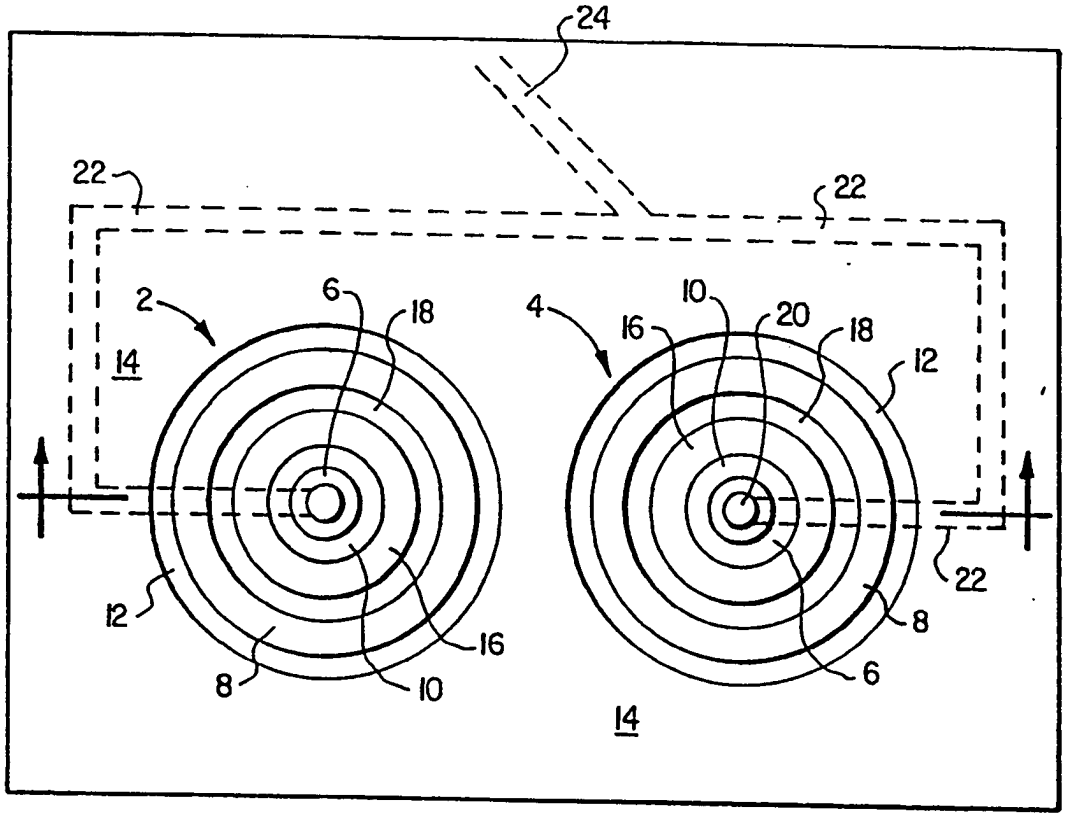
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FIG. 1

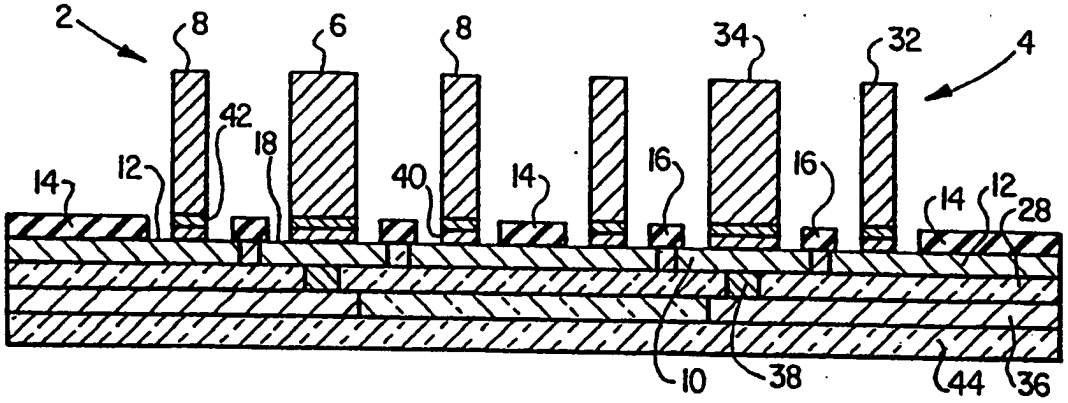
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FIG. 2

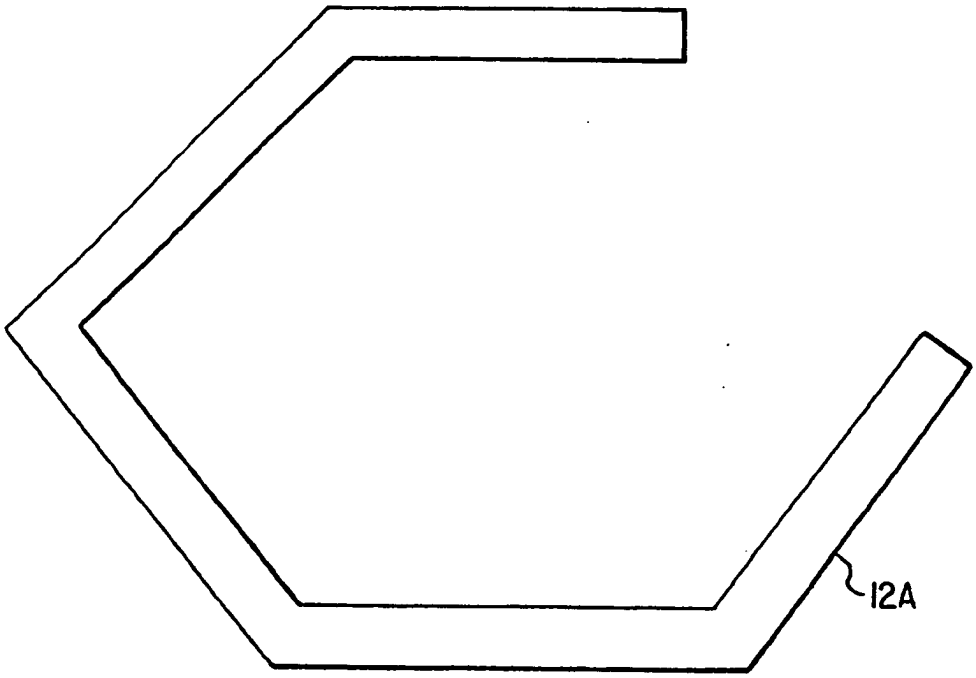

FIG. 3

COAXIAL DIE AND SUBSTRATE BUMPS

U.S. GOVERNMENT LICENSE RIGHTS

The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of Contract No. MDA904-90-C-5285 awarded by the Maryland Procurement Office.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuit fabrication and, more particularly, to structures and methods for interconnecting dies and substrates.

2. Description of Related Art

In many applications, it is necessary to provide intimate contact between a semiconductor device and the substrate to which it is mounted. Intimate contact is needed to assure a sufficient electrical connection and also sufficient thermal conductivity.

One example of the foregoing "applications" involves multilayer ceramic (MLC) technology. To overcome the limitations and the expense of MLC technology for high-performance systems, silicon wafers have heretofore been used as substrates for thin-film interconnection modules. Such silicon PC boards (SiPCBs) can provide very precise, high-density interconnects with a minimal number of metal levels. With sufficient metallization thickness, near transmission-line quality interconnects have been achieved over wafer-scale distances. SiPCBs also have very good thermal and mechanical characteristics; for example, they are virtually immune to thermal stresses, owing to the thermal expansion match between the chips and the board.

In order to physically attach and then electrically connect IC chips to a silicon wafer, three standard techniques have been successfully adapted from ceramic hybrid technology: flip-chip solder-bump reflow, wire bonding, and tape-automatic-bonding (TAB). The first listed of these methods, the solder bump method, is most relevant to the present invention. In this method, alternative layers of conductor and ceramic insulator are pressed together in the green state and fired to form a multilayer structure. Chips are provided with solder bumps on each pad and subsequently mounted upside down so that the solder bump positions on the chip correspond to interconnect areas on the ceramic multilayer.

It should not be forgotten that a main goal of the foregoing methods is to promote high speed devices. Reduced circuit dimensions act towards fulfillment of this goal. That is, to promote speed, it is desirable to interconnect chips with a minimum of capacitive loading and a minimum of interconnect length. Capacitive loading tends to slow down signal transmission such that high speeds attained on the chip cannot be maintained in communicating from one chip to another. Interconnection length between chips also contributes to propagation delay due to circuit length and also due to a self-inductance of the interconnection circuit.

Increasingly higher signal speeds have caused electrical problems to arise in the chip or die to substrate interface. These problems are particularly notable with greater than 250 MHz signals and in systems having both digital and analog signal components. Specifically, it has been found to be extremely difficult to minimize crosstalk between adjacent signal bumps and to maintain constant transmission line impedance as high speed signals traverse the interface of a die and substrate through a bump.

As bump construction plays a significant role in the present invention, some discussion of solder bump structure is appropriate here. Uniaxial solder bumps have been in use for many years and have found applicability in a wide variety of semiconductor chip to substrate or printed circuit board input/output (I/O) connections. Applications have been exploited in both the analog and digital interface areas. As technological advances have been and are continuing to be made in electronic systems with regard to higher frequency in analog applications and higher clock speed in digital systems, the standard uniaxial solder bump has been and continues to become an increasingly limiting portion of structures, especially with regard to crosstalk and impedance control. Additionally, there are emerging combined analog/digital hybrid systems where attractive applications for high speed signal processing exist but low crosstalk is essential at signal I/O's. Low crosstalk signals are extremely important where disparate signal levels are communicated via adjacent bumps. These situations arise in a variety of analog applications and in digital circuits where data signals are close to clock distribution bumps and power supply distribution bumps.

Thus, chip-to-board interconnection technology appears to be a weak point in terms of electrical performance and mechanical reliability of silicon hybrid wafer scale integration technology. It is a shortcoming and deficiency of the prior art that stringent requirements of low crosstalk and controlled impedance are not satisfactorily addressed by prior art solder bump interconnection methods.

SUMMARY OF THE INVENTION

The present invention overcomes the shortcomings and deficiencies of the prior art by providing a coaxial bump I/O configuration between die and substrate. More specifically, the present invention provides a coaxial bump for connecting a die to a substrate. The coaxial bump includes a center post and a ground ring surrounding the center post. In embodiments of the present invention the center post may be a center conductor line. In the same or in other embodiments of the present invention, the ground ring may be at least generally torus-shaped.

In addition, neither a complete ground ring nor a complete bond are necessarily required for adequate electromagnetic shielding, depending on the application. In fact, a gap or gaps in the ground ring may be desirable for allowing gas pressure release during bonding without significantly decreasing the ground ring's electromagnetic shielding capability. For example, the ground ring may have a hexagonal layout with one of the six sides removed.

The present invention also provides a method for bonding a die to a substrate including the steps of providing the substrate with a coaxial bump, providing the die with a coaxial bump, and connecting the coaxial bump on the substrate to the coaxial bump on the die. In embodiments of the method of the present invention the coaxial bumps may be at least partially formed with indium. In the same or in other embodiments of the method of the present invention, the connecting step

may be accomplished by welding, at room or elevated temperature, and/or in an inert atmosphere.

Accordingly, it is an object of the present invention to provide a coaxial solder bump configuration that satisfies even the most stringent requirements for low crosstalk and controlled impedance at a die to substrate interface.

Another object of the present invention is to provide a solder bump configuration that clears the way for increasingly higher speed signal processing.

Yet another object of the present invention is to provide a die to substrate interface in which maintenance of accurately controlled impedances over a wide frequency range is possible.

Still yet another object of the present invention is to provide a die to substrate interface having a shielded center post. The shield, which may be either nearly closed or completely closed, permits only a very low level of crosstalk between the center post and adjacent signal bumps.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, advantages, and novel features of the present invention may best be understood by reference to the following description taken in connection with the accompanying drawings in which:

FIG. 1 is a top view of two coaxial bumps in a daisy chain section according to the teachings of the present invention;

FIG. 2. is a cross-sectional view of the coaxial bumps shown in FIG. 1 taken along line 2—2 and

FIG. 3 is a cross-sectional view of a ground ring having a hexagonal layout with one of the six sides removed.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings wherein like reference numerals are used to designate identical or similar elements throughout the several views, and wherein elements are not necessarily shown to scale, and more particularly to FIG. 1, there is shown a top view of a coaxial bump according to the teachings of the present invention. More precisely, there is shown in FIG. 1 a first bump 2 and a second bump 4 connected by a daisy chain section.

Bumps 2, 4 each comprise an inner solder bump 6 and an outer solder bump 8. Surrounding the bumps 6 and 8 are a niobium inner pad 10 and a niobium ground plane section 12, respectively. The niobium ground plane section 12 is seen through a hole in outer passivation layer 14. An inner extent of passivation shown as inner passivation 16 surrounds niobium inner pad 10, and inner niobium ground plane ring 18 is located between passivation 16 and outer bump 8. At the center of all of the foregoing is a center post via feed 20 inside inner bump 6.

Those skilled in the art should appreciate that the coaxial bump shown in FIG. 1 is effectively and essentially a donut-shaped ground ring surrounding a center post. The center post is a center conductor line surrounded by an outer ground shield.

Coaxial configurations have heretofore been used for transmission lines in microwave applications; however, perhaps because of the perceived and real difficulties encountered in fabricating such structures at a useful size for solder bump applications, the inventors of the present invention are aware of no attempts or conception of using such configurations in the art relevant hereto.

Coaxial bumps such as those shown in FIG. 1 have been fabricated and bonded by the inventors of the present invention. This demonstration of feasibility involved a superconducting substrate rendered in niobium conductors with silicon dioxide dielectric which was fabricated using indium bumps which were diffusion bonded at elevated temperature. Furthermore, it is understood that other conductors such as copper and aluminum and other dielectrics such as polyimide can be employed in the coaxial bumps of the present invention.

Continuing to refer to FIG. 1, the daisy chain section previously mentioned as connecting left coaxial bump 2 and right coaxial bump 4 may be seen to comprise a daisy chain connection 22 between the two inner bumps 6. Connection 22 has an associated lead 24 that is connected to test pads on the substrate.

In a preferred embodiment of the present invention, a superconducting substrate using niobium conductors and a silicon dioxide inner layer dielectric may be built up using a planarized via technology with a desired, pre-determined number of layers as shown for clarity in FIGS. 1 and 2. The final top layer is the niobium ground plane 12 which is applied between a silicon dioxide layer 28 and a passivation layer 30 which includes inner passivation 16 and outer passivation 14. The ground plane may completely cover the top surface of the substrate beneath passivation 30 except where the coaxial bump's inner conductor feeds through the surface to accept a bump. The outer bump shield 32 is electrically connected to ground plane 12 while the inner conductor 34 is electrically isolated from it. A niobium line 36, which feeds to the inner conductor 34, is routed through a via 38 in the top dielectric 28 to the small niobium pad 10 which is isolated from the main niobium ground plane 12. Thus, the niobium feed line passes under the outer coaxial bump pad 32 separated electrically from the ground plane 12 by a layer of silicon dioxide 28. The dimensions of the feed line 36 (that is, its width and thickness) are chosen to yield the proper strip line impedance.

The exposed, top niobium strip line pads are metallized with a so-called barrier metal (e.g., about 2,000 angstroms thick) of palladium 40 which is solderable with indium. A thin, gold layer (e.g., also about 2,000 angstroms thick) 42 is applied to the whole surface of the wafer to act as an electrical plating interconnect and ultimately a metallic flux (due to its extreme solubility in indium) for wetting and alloying the indium to the palladium. A thick (e.g., from about 15 to about 30 microns thick) photoresist mask is applied to the gold surface, then is used as a plate up mask for plating 15 micron high indium bumps in the coaxial configuration. The thick, resist mask is stripped and the indium bump is used as a mask for etching the gold interconnect in a gold etchant which does not attack the indium bump. Underlying the entire structure shown in FIG. 2 is another silicon dioxide layer 44.

In another preferred embodiment of the present invention, which is not shown, a non-planarized structure can be built up using an alternating via technology with identical functionality to the planarized version.

The presently preferred bonding method is by cold weld where both die and substrate are bumped and indium is forced to flow against indium to effect a weld at room temperature. In this configuration, the indium

bumps are reduced in height from by about 25 to 50 percent during the pressure weld operation to ensure substantial cold flow of the indium at the surface. A conventional indium oxide etchant is used just before bonding to remove the native indium oxide on the bumps to ensure cleaner weld interfaces. The actual bonding is accomplished in an inert environment to further reduce the chance of indium oxidation during the bump operation. It is understood, however, that the bumps on the die and the substrate may be connected by other conventional techniques, including a warm welding, adhesive bonding, thermosonic bonding and thermalcompression bonding. Furthermore, the bumps may be of other materials such as aluminum.

In the practice of the present invention, there is essentially no lower limit to the pitch and size of the coaxial bumps which can be made. There are, however, limits to the lithography machines used to print the bump plate-up mask which occur when the lateral dimensions of the bump approach current IC fabrication limits. Similar limits in resolution preclude bump heights of more than the lateral dimensions (that is, aspect ratios of bump heights to width of less than about one to one). Other limits are found in the positioning accuracy of the bonding tool which may be on the order of a few microns and limits on the flatness of the substrates upon which the bumps are placed. With all of these current limitations, at the present time it appears possible to fabricate coaxial bumps with diameters as small as 10 microns.

Those skilled in the art should appreciate that the present invention provides a number of novel features and advantages. For example, the present invention allows the maintenance of accurately controlled impedance through a bumped interface over a wide frequency (e.g., 20 GHz or more). The low impedences made possible by coaxial bumps also eliminates concerns with "di/dt" inductive noise in power supplies (although similar results may be possible with an array of ground bumps surrounding the supply bump). Furthermore, the nearly or completely closed nature of the shielded bump provides for a very low level of crosstalk between the shielded bump and adjacent signal bumps. This allows packing many IO's together while keeping crosstalk between them low. This latter point is an important advantage of the present invention: that is, it allows highly controlled impedances and low crosstalk at chip IO's.

The standard impedance formula for coaxial lines is:

$$Z_o=(1/\pi) * sqrt(\mu/\epsilon) * ln(r_b/r_a)$$

where Z_o is the impedance, μ is the permeability of the dielectric, ϵ is the permittivity of the dielectric, r_a is the outer radius of the inner bump and r_b is the inner radius of the outer shield. Using the standard impedance formula, the impedance of a coaxial bump of the present invention can be calculated to be:

$$Z_o=60 * ln(r_b/r_a)$$

Thus, for example, a coaxial bump of the present invention which is placed between the pads of a die and a substrate with $r_b=2.3 * r_a$ can exhibit a line impedance of about 50 ohms.

Obviously, numerous modifications and variations are possible in view of the above teachings. For example, discussed above is the fabrication of a superconducting substrate rendered in niobium conductors with a silicon dioxide dielectric using indium bumps which were diffusion bonded at an elevated temperature. Other die and substrate materials can be used with rather trivial changes in barrier metallurgical layers as an accommodation between bump solder and the interconnect metal. For example, copper/polyimide substrate systems can be attached to silicon MOS, bi-polar, or GaAs device types, for instance by flip-chip bonding. Furthermore, coaxial bumps (and uniaxial bumps) at least partially formed with aluminum can be connected together, such as by a fluxless aluminum weld with ultrasonic energy. The weld may be a warm weld (e.g., at 250° C.) or a cold weld (e.g., at room temperature). A fluxless weld would eliminate the need for removing residual flux within a cavity, which is particularly advantageous in the case of a closed cavity. Moreover, flip-chip bonding a die with aluminum pads to a substrate with aluminum bumps may quite possibly yield enormous economic advantages for both coaxial and uniaxial pads and bumps. Still further, as mentioned in the summary of the invention section above, a gap or gaps in the ground ring may be desirable for allowing gas pressure release during bonding without significantly decreasing the ground ring's electromagnetic capability. For example, as shown in FIG. 3, a ground ring 12A may have a hexagonal layout with one of the six sides removed. Accordingly, within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described hereinabove.

What is claimed is:

1. A coaxial bump for connecting a die to a substrate, said coaxial bump comprising:
   a center conductor line; and
   a ground ring spaced from and surrounding said center conductor line wherein said ground ring provides said center conductor line with electromagnetic shielding from adjacent signal bumps thereby permitting only a very low level of crosstalk between said center conductor line and said adjacent signal bumps.

2. A coaxial bump as recited in claim 1, wherein said ground ring is at least generally torus-shaped.

3. A coaxial bump as recited in claim 2, wherein said ground ring completely surrounds said center conductor line.

4. A coaxial bump as recited in claim 3, wherein said bump contains no flux within said ground ring.

5. A coaxial bump comprising:
   a dielectric layer;
   a passivation layer;
   a ground layer disposed between said dielectric layer and said passivation layer;
   an inner bump center conductor extending through and electrically isolated from said ground layer; and
   an outer bump shield mounted atop and electrically connected to said ground layer.

6. A coaxial bump as recited in claim 5, wherein said dielectric is selected from the group consisting of silicon dioxide and polyimide.

7. A coaxial bump as recited in claim 5, wherein said ground layer is selected from the group consisting of niobium, copper and aluminum.

8. A coaxial bump as recited in claim 5, further comprising a feed within said dielectric layer connected to

said inner bump center conductor and electrically isolated from said ground layer.

9. A coaxial bump as recited in claim 8, further comprising exposed, top stripline pads.

10. A coaxial bump as recited in claim 9, wherein said exposed, top stripline pads are metallized with a barrier metal.

11. A coaxial bump as recited in claim 10, wherein said barrier metal is palladium.

12. A coaxial bump as recited in claim 9, wherein said entire coaxial bump is formed on a wafer.

13. A coaxial bump as recited in claim 12, wherein said wafer has a surface which is coated with gold so as to provide a plating interconnect.

14. A coaxial bump for connecting a die to a substrate, said bump comprising:

a center conductor line; and

a ground ring with at least one gap therein, said ground ring spaced from and partially surrounding said center conductor line wherein said ground ring provides said center conductor line with electromagnetic shielding from adjacent signal bumps thereby reducing crosstalk between said center conductor line and said adjacent signal bumps.

15. A coaxial bump as recited in claim 14, wherein said at least one gap does not significantly decrease the electromagnetic shielding capability of said ground ring.

16. A coaxial bump as recited in claim 15, wherein said at least one gap permits gas pressure release.

17. A coaxial bump as recited in claim 15, wherein said die is flip-chip bonded to said substrate.

18. A coaxial bump as recited in claim 15, wherein said center conductor line is at least partially formed with aluminum.

* * * * *

US005442144A

United States Patent [19]

Chen et al.

[11] Patent Number: 5,442,144

[45] Date of Patent: Aug. 15, 1995

[54] MULTILAYERED CIRCUIT BOARD

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Related U.S. Application Data

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[51] Int. Cl.[6] H05K 1/00

[52] U.S. Cl. 174/266; 174/250; 174/260; 174/262; 361/784; 361/792

[58] Field of Search 174/250, 251, 260, 261, 174/262, 263, 264, 265, 266; 361/784, 785, 790, 792

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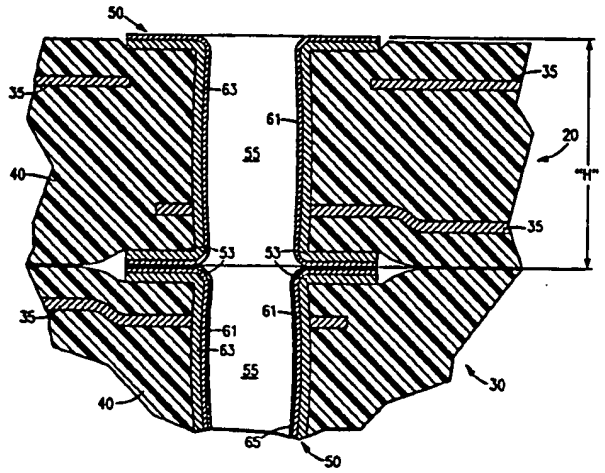
[57] ABSTRACT

A method of making a multilayered circuit board wherein at least two layered subassemblies, each comprising a dielectric layer and at least one conductive layer therein, are bonded together. Each subassembly includes a through-hole extending therethrough which is aligned with a respective through-hole of the other prior to bonding. The subassemblies are compressed at a predetermined pressure (e.g., 300 psi) and then heated to a first temperature (e.g., 300° C.) for an established time period, resulting in formation of a bond between the two through-holes. The resulting alloy formed from this bond possesses a melting point significantly greater than that of the subassembly dielectric (e.g., PTFE). Following this time period, the compressed subassemblies are heated to an even greater temperature (e.g., 380° C.), again for an established time period, to assure dielectric flow. The subassembly is then cooled and the pressure removed. The method possesses two significant features: (1) effective engagement between respective pairs of through-holes in the compressed subassemblies; and (2) prevention of dielectric incursion within the bond formed between the respective pairs of through-holes, which incursion could adversely affect the electrical connection therebetween.

7 Claims, 5 Drawing Sheets



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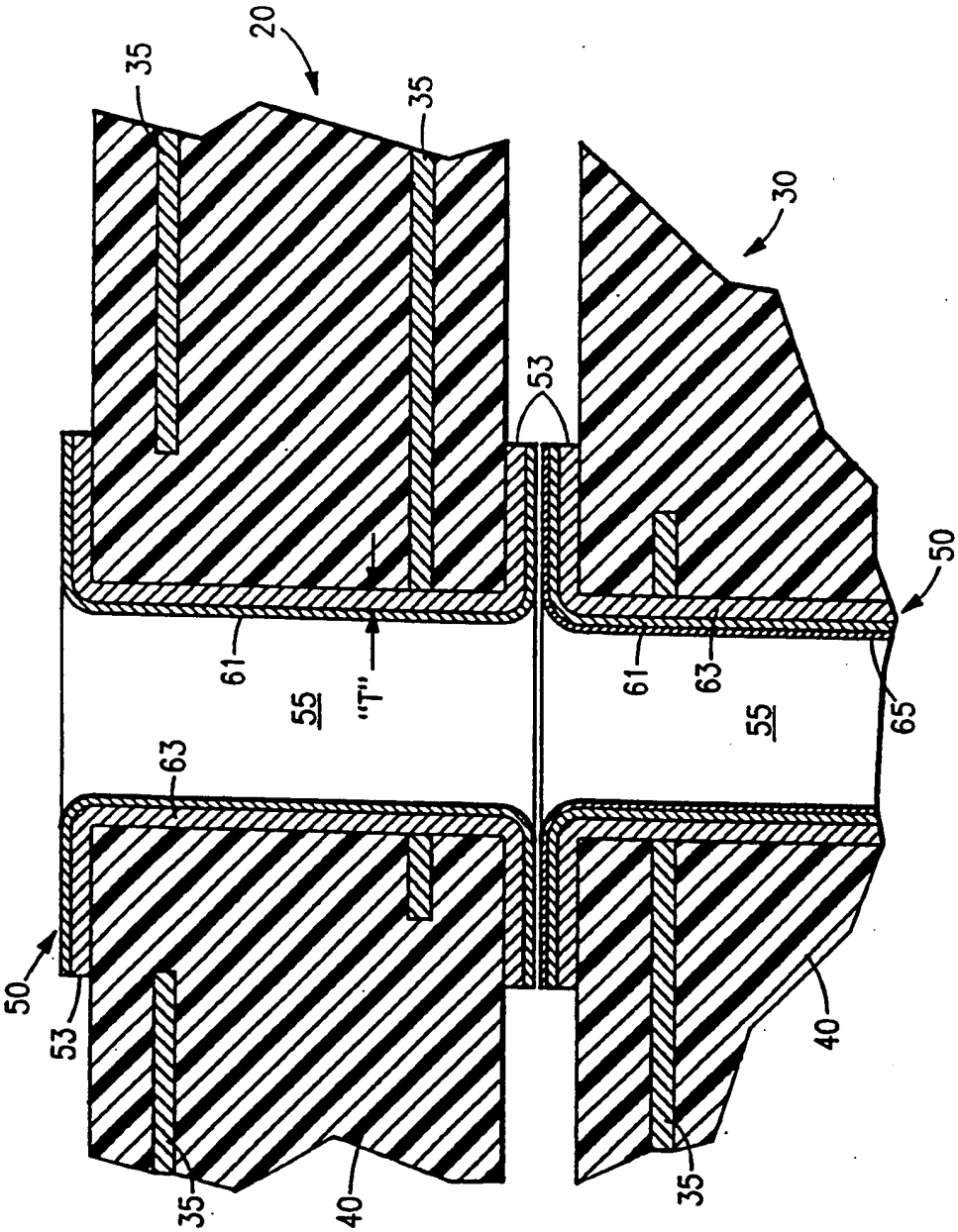

FIG.1

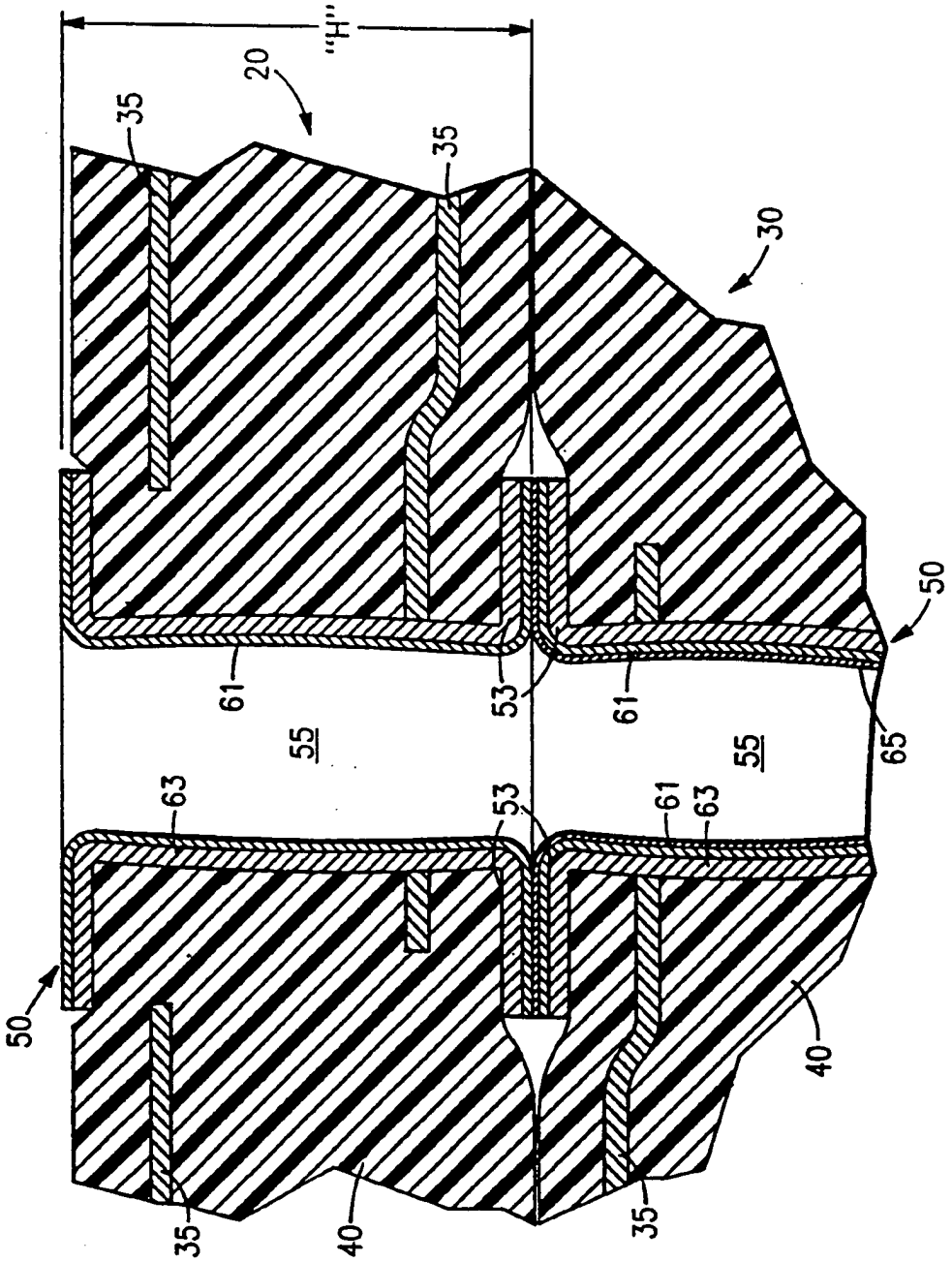

FIG.2

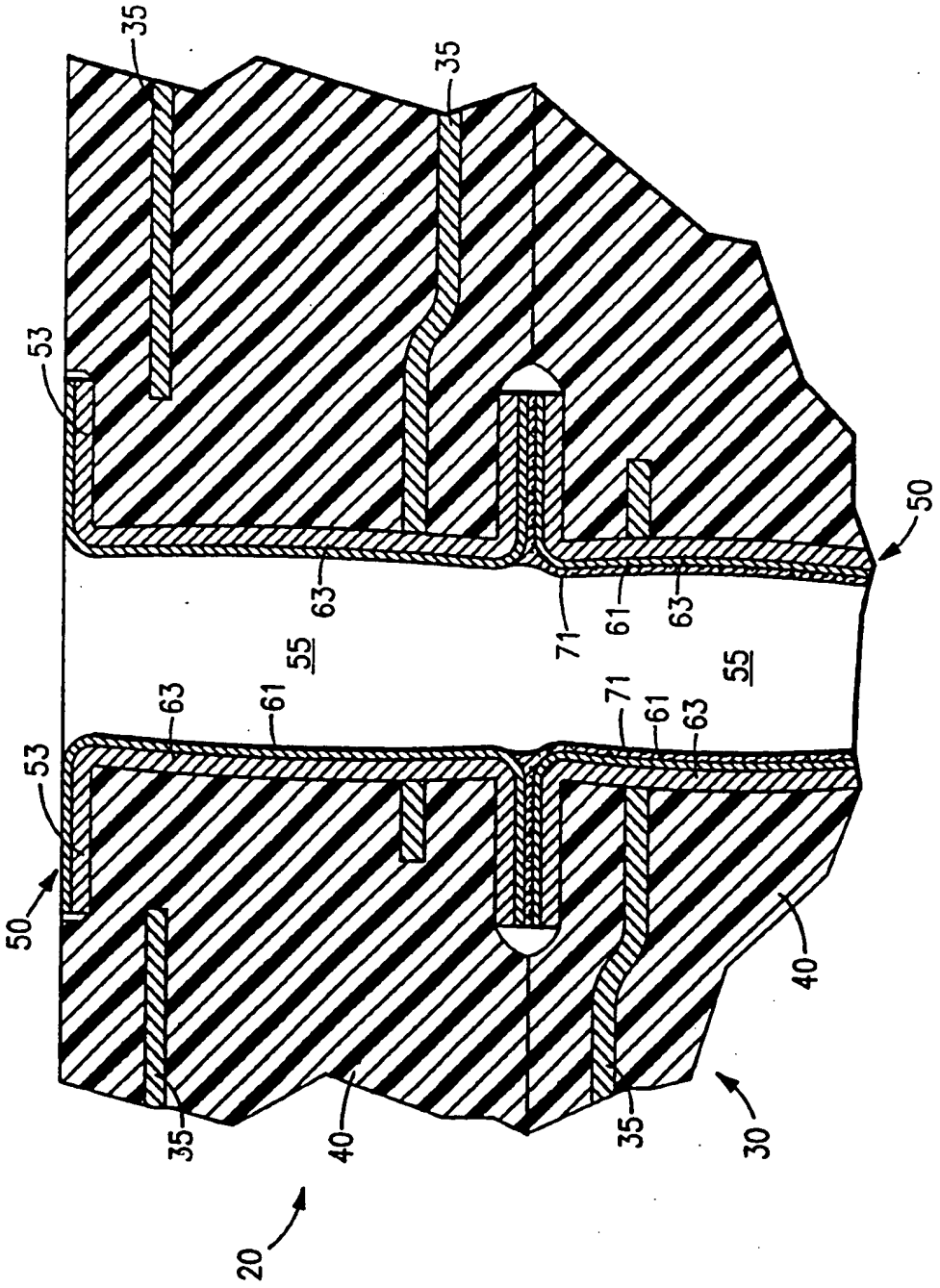

FIG.3

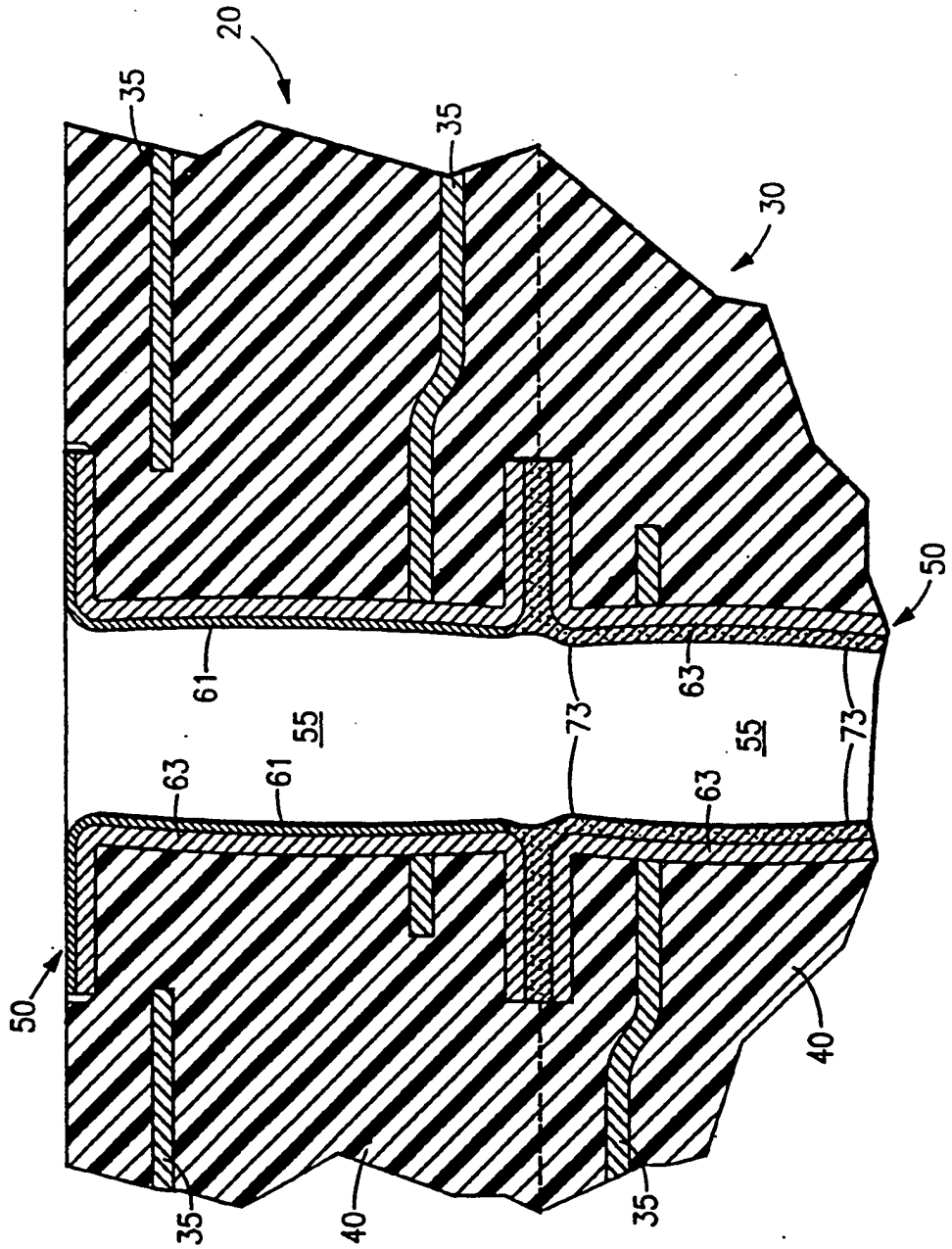

FIG.4

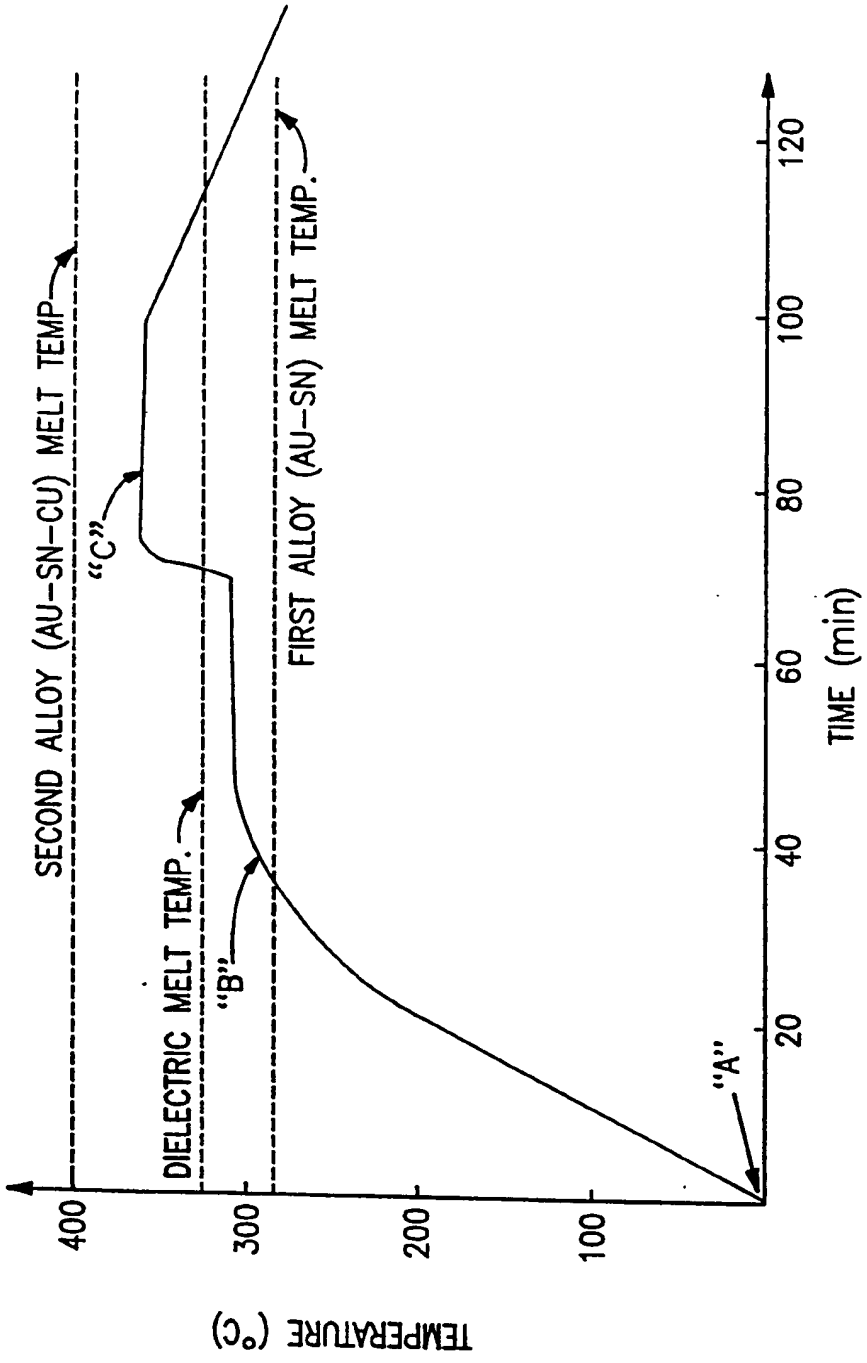
SECOND ALLOY (AU-SN-CU) MELT TEMP
"C"
DIELECTRIC MELT TEMP.
"B"
FIRST ALLOY (AU-SN) MELT TEMP.
"A"
400
300
200
100
TEMPERATURE (°C)
20
40
60
80
100
120
TIME (min)

FIG.5

MULTILAYERED CIRCUIT BOARD

CROSS REFERENCE TO CO-PENDING APPLICATIONS

This application is a divisional of Ser. No. 08/112,499 filed Aug. 26, 1993, now U.S. Pat. No. 5,359,767. In Ser. No. 07/536,145, entitled "Au-Sn Transient Liquid Bonding In High Performance Laminates" and filed Jun. 11, 1990, there is defined a method for simultaneously laminating circuitized dielectric layers to form a multilayered, high performance circuit board. Two metals are chosen to form an initial eutectic layer that, when solidified, forms an alloy bond that will only remelt at a second temperature greater than that causing the eutectic bond. Once solidified, the alloy is designed to remain solid throughout subsequent laminations. The teachings of this filed application are incorporated herein by reference. Ser. No. 07/536,145 is now U.S. Pat. No. 5,280,414, having issued Jan. 18, 1994.

TECHNICAL FIELD

The invention relates to printed circuit boards, and particularly those of the multilayered variety.

BACKGROUND

Multilayered printed circuit boards, including those referred to as of the high density variety, are typically constructed of several electrically conductive layers separated by layers of dielectric material. Some of the conductive layers may be utilized as power and ground planes while other conductive layers may be patterned for electrical signal connections (e.g. between integrated circuit chips). Layer-to-layer interconnections may be used in such constructions and accomplished using what is referred to as plated-through-holes (PTH's), such holes typically including a plating of electrically conductive material (e.g., copper) thereon. In those situations wherein electrical interconnections are desired between adjacent conducting layers, it has been common in the art to provide such connections with what are often referred to as "vias". These hole-type connections, though typically not extending through the entirety of the board's thickness, are also coated (e.g., plated) with an internal conductive layer (e.g., copper). Such "vias" and through-holes are typically provided by drilling.

The term "through-hole" as used herein is meant to include the aforementioned PTH's as well as "vias" that may only interconnect selected conductive layers in the final structure (and thus possibly be only internally positioned).

Examples of various types of multilayered printed circuit board (PCB) constructions are defined in U.S. Pat. Nos. 4,030,190 (K. Varker), 4,554,405 (K. Varker), 4,854,038 (J. Wiley), 4,864,772 (D. Lazzarini et al.), 4,868,350 (J. Hoffarth et al.) and 5,191,174 (C. S. Chang). All of these patents are assigned to the same assignee as the instant invention. Additional examples, including those which describe various steps in producing such final composite structures, are shown in U.S. Pat. Nos. 4,803,450 (J. Burgess), 5,046,238 (R. Daigle) and German Patent DE3316017 (M. Bergmann).

As defined in the above and other patents, and as is also well known in the art, such multilayered printed circuit board constructions typically utilize copper or a similar highly conductive material for the signal and/or power and/or ground conductive planes. The term "printed circuit board" as used herein is thus meant to define a structure including at least one dielectric layer and at least one conductive layer located therein and/or thereon. One well known example of a dielectric material for use in such construction is fiberglass reinforced epoxy resin (aka FR4). Other materials may include polyimide and polytetrafluoroethylene (PTFE), the latter of more recent vintage when relatively low dielectric materials are desired. As will be understood from the following, the teachings of the present invention are especially adaptable to multilayered PCB's wherein PTFE or the like is used as the dielectric material and copper is used as the conductive (metal) material for the various through-holes and conductive layers used therewith.

As defined herein, the present invention comprises a method of making a multilayered circuit board construction comprised of individual layered subassemblies each including electrically conductive wiring and at least one through-hole therein. The resulting multilayered structure as defined herein is characterized by the provision of at least two of these subassemblies being bonded together such that respective through-holes of each are aligned, engaged, and coupled through formation of a metallurgical bond at the through-hole jointure. Such a bond is achieved through the unique use of heat and pressure, and precise quantities of selected metals (e.g., gold and tin) in the jointure location. Significantly, the through-holes are of a pre-established configuration with precisely defined (in thickness) sidewalls that, uniquely, allow at least partial compression (collapse) of the sidewalls during pressure application at a designated temperature. Such compression, possible by several such paired through-hole combinations, assures effective engagement therebetween so that sound electrical connection is made possible across the entire final PCB structure.

Still further, the method defined herein results in formation of the aforementioned metallurgical bond while also, uniquely, providing a resulting alloy at the through-hole jointure that possesses a melting point much greater than that of the initial eutectic alloy formed. Most significantly, this new melting point is also greater than the corresponding melting point of the dielectric materials (e.g., PTFE) used in each layered subassembly being so bonded. This unique result enables subsequent heating of the initially bonded subassemblies to an elevated temperature above the dielectric's melting point, resulting in dielectric flow as desired. Because the formed alloy remains in the solid state during such dielectric flow, the heated dielectric material is prevented from migrating or otherwise moving into the through-hole jointure and thereby possibly adversely affecting the electrical connection formed at this location.

The present invention thus represents an improvement over the process defined in U.S. Pat. No. 5,280,414, as well as those processes mentioned in U.S. Pat. Nos. 4,803,450 and 5,046,238 and German patent DE3316017, and is thereby deemed to constitute a significant advancement in the art.

DISCLOSURE OF THE INVENTION

It is, therefore, a primary object of the present invention to enhance the art of multilayered circuit boards.

It is a particular object to provide a method of making a multilayered circuit board wherein effective en-

gagement between aligned through-holes of adjacent layered subassemblies being bonded to form part/all of the final board structure is assured.

It is a further object to provide such a method which will further assure effective dielectric flow (melt) during application of pressure at a selected temperature, while effectively preventing dielectric material from adversely affecting the through-hole jointures which serve to provide critical paths for electrical current flow in the finished product (PCB).

In accordance with one aspect of the invention, there is defined a method of making a multilayered circuit board assembly which includes at least two layered subassemblies each including at least one dielectric layer, electrically conductive wiring in the form of at least one conductive layer and at least one conductive through-hole therein. The method comprises the steps of aligning the layered subassemblies relative to one another such that at least a first of said conductive through-holes of one layered subassembly is aligned with and engages a second conductive through-hole in a second layered subassembly, the first and second conductive through-holes including a layer of first metal thereon, said second conductive through-hole further including a layer of second metal thereon. These subassemblies are subjected to pressure at a level sufficient to cause at least partial compression of the first and second conductive through-holes, following which the layered subassemblies are heated to a pre-established temperature for a predetermined time period sufficient to form a metallic bond between the first and second metals on the conductive through-holes. The layered subassemblies are then cooled.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-4 represent the various steps of making a multilayered circuit board assembly in accordance with one embodiment of the invention, these views illustrating at least two layered subassemblies which will comprise the final assembly; and

FIG. 5 is a time vs. temperature graph illustrating the sequence of steps of the invention as represented in FIGS. 2-4, FIG. 5 also illustrating examples of the melting points of various materials used in the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

For a better understanding of the present invention, together with other and further objects, advantages and capabilities thereof, reference is made to the following disclosure and appended claims in connection with the above-described drawings.

The following disclosure and associated drawings define a process for making a multilayered circuit board assembly possessing the unique characteristics defined herein. As understood, this final assembly will include a plurality of layered subassemblies joined together in a predetermined manner such that respective ones of these will possess the operational characteristics (wiring density, resistance) defined.

In FIGS. 1-4, there are shown the various steps of making a multilayered circuit board assembly in accordance with one embodiment of the invention. These FIGS. illustrate one example of a layered subassembly 20 capable of being combined with another layered subassembly 30 to form the multilayered circuit board of the invention. It is to be understood that the configuration depicted in these FIGS. is representative of only one version of such subassemblies and the invention is thus not limited thereto. In the simplest form of the invention, it is to be understood that each layered subassembly as used herein will include at least one dielectric layer 40 and attached or internally contained singular conductive layer 35. By the term conductive layer as used herein is meant to include a singular layer of electrically conductive material (the preferred material being copper), said layer capable of functioning as a signal, power or ground layer, or combinations thereof. The term "compression" as used herein is meant to define a condition of reduced height for the invention's through-holes as a result of being subjected to pressures typically associated with such processes as lamination. Under such definition, it is understood that some deformation must occur.

It is further understood that each layered subassembly may include additional conductive layers, depending on the operational requirements of the final circuit board assembly. In one example, it may be possible to utilize a total of about ten such conductive layers, strategically positioned in accordance with a predefined pattern. In the drawings, two such conductive layers 35 are shown for the layered subassembly 20.

Additionally, it is also within the scope of the present invention to produce a multilayered circuit board assembly having more than two layered subassemblies. By way of example, it is possible, using the unique teachings of the present invention, to produce a multilayered assembly including twenty individual layered subassemblies as part thereof. Significantly, the method defined herein is readily capable of being utilized to provide such a multilayered and complex structure.

As stated above, the invention is particularly adapted for use with PTFE or the like dielectric materials, as well as conductive layers comprised substantially of copper. Further, the invention is particularly adapted for use with through-holes (defined in greater detail hereinbelow) comprised substantially of copper as the primary conductive material, this copper further including a layer (e.g., plating) of precious metal (e.g., gold) thereon. As further defined herein below, at least one of these conductive through-holes will include a second layer (e.g., plating) of another metal (preferably tin). The present invention is not to be limited to these particular materials, however, in that other materials may be utilized quite successfully.

As defined herein, the method of the present invention comprises a singular process wherein both lamination and interconnection occur between at least two layered subassemblies to produce the final multilayered structure. Each subassembly is capable of being individually tested and/or repaired prior to final lamination and connection with respective additional subassemblies. Additionally, it is also within the scope of the invention to individually test and/or repair respective pairs of such laminated and connected subassemblies prior to incorporation thereof within additional layered elements to form the final structure. Such testing and/or repair possibilities greatly enhance the yield in the final product while also serving to substantially shorten process time and assure overall cost savings. The present invention also permits the construction of multi-layered assemblies with extremely high aspect ratio (height to diameter)through-holes. The invention thus represents a significant advancement in the art.

As will be defined herein below, the invention utilizes what is referred to as transient liquid bonding (TLB), which, as defined in the aforementioned U.S. Pat. No. 5,280,414, is a diffusion bonding process which involves the deposition of different conductive surface metals which together are then capable of forming a eutectic melt. The surfaces being bonded must be comprised of highly conductive metal, such as copper, and coated with the metals, brought into physical contact with one another and then heated above the eutectic temperature, the resulting interdiffusion thereby forming a melt. Solidification of this liquid region through further diffusion results in bonding of the metallic surfaces. Significantly, the TLB process does not require the use of flux and may utilize minimal amounts of solder. Bridging between adjacent bonding surfaces is reduced in comparison to conventional soldering processes. Most significantly, it is understood from the teachings herein that the present invention, while utilizing the advantages of the TLB process as defined in U.S. Pat. No. 5,280,414, represents a significant improvement over the method in said application and thus represents an advancement in the art. Again, the teachings of U.S. Pat. No. 5,280,414 are incorporated herein by reference.

In FIG. 1, each of the individual layered subassemblies 20 and 30 is shown to include at least one through-hole 50 which forms a part thereof. As shown, each through-hole extends through the entire thickness of the PTFE dielectric 40 and includes opposing, external land segments 53 as part thereof. Preferably, dielectric 40 also includes a filler material (e.g., silicon dioxide in particle form). (The lower land segment for subassembly 30 is not shown but understood to exist.) These outwardly extending land segments 53 project from a centrally-located hollow cylindrical portion 55 of the through-hole and, in initial orientation (FIG. 1), are located on the respective opposing outer surfaces of the interim dielectric. Each through-hole is preferably comprised of copper or similarly conductive metal as is known in the art. Significantly, each through-hole is of hollow construction.

Although only one through-hole is shown for each layered subassembly, it is fully understood that the invention is not limited to this number in that, in a preferred embodiment of the invention, several such through-holes are utilized. In one embodiment of the invention, for example, a total number of about 10,000 such through-holes may be provided per subassembly, for alignment with and engagement to a respective, similar number of such through-holes in the other subassembly.

In a preferred embodiment, the copper material for each through-hole possesses a thickness of only about 0.3 mils. Such a thickness is represented by the letter "T" in FIG. 1. The above thickness is not meant to limit the invention, however, in that other thicknesses are possible. In a layered subassembly having an overall dielectric thickness of about nine mils, and using through-holes having a central hollow cylindrical portion with an external diameter within the range of from about three mils to about ten mils, total copper thicknesses within the range of about 0.2 mils to about one mil may be successfully utilized. These parameters are considered critical with respect to the present invention due to the requirement that these conductive through-holes at least partially compress during the initial phases of producing the multilayered circuit board defined herein. Such partial compression is deemed significant to assure proper engagement (and therefore electrical coupling) between many respective pairs of such elements, thereby compensating for possible lack of planarity in the respective dielectric portions of each subassembly. Because the desired conductive paths in the final multilayered structure are through these engaged pairs, including from opposing surfaces thereof to various internal conductive layers such as shown herein, such positive connection between respective pairs of such elements is absolutely essential to the successful operation of the final product.

In FIG. 1, subassemblies 20 and 30 are aligned such that the respective land portions 53 of through-holes 50 are precisely aligned relative to one another. Significantly, the upper through-hole in FIG. 1 includes a layer of first metal (61) thereon, which metal is, of course, in addition to the copper which forms the lands 53 and cylindrical body portion 63. In a preferred embodiment, each first metal 61 (both through-holes including this metal) is preferably gold and is provided (e.g., plated) of a thickness of from about 0.12 mils to about 0.32 mils. When using copper having a thickness of 0.30 mils, the gold preferably has a thickness of 0.24 mils, thus slightly thinner than the copper. The gold layer 61 in subassembly 30 is of similar thickness.

In addition to the above first layers on the copper, the lower throughhole of subassembly 30 further includes a second additional metal, preferably tin. This layer is represented by the numeral 65 in FIG. 1. As defined in U.S. Pat. No. 5,280,414, this tin eventually forms a eutectic alloy with the gold during the TLB process, this to be defined in greater detail hereinbelow.

The tin layer of 65 may have a thickness of from about 0.04 mils to about 0.16 mils, and is preferably of a thickness of 0.10 mils when using 0.30 mil copper and 0.24 mil gold.

Alignment of the two subassemblies 20 and 30 is preferably accomplished using techniques known in the art and further description is not deemed necessary.

In FIG. 2, both layered subassemblies are shown as being engaged and appropriate pressure applied. In a preferred embodiment, such engagement occurs at room temperature and at a pressure of from about 200 pounds per square inch (psi) to about 400 psi. In a preferred embodiment, this pressure was 300 psi. Dimensions of the plated through conductive metal in the preferred embodiment have been selected to provide a controlled compressibility under such pressures. As shown, this compressibility results in a full interface contact between respective facing surfaces of the land portions 53 of each through-hole, thereby assuring effective connection therebetween. Understandably, such connections occur at all paired through-hole locations in these combined subassemblies. As seen in FIG. 2 (and FIGS. 3 and 4), the sides walls of the hallow cylindrical portion 55 are of curved configuration.

Most significantly, each through-hole at least partially compresses to a reduced overall height (dimension "H" in FIG. 2) slightly less than that prior to compression. In one embodiment, wherein the through-holes of the materials and thicknesses described above were utilized, this resulting reduction in overall height was within the range of from about ten percent to about twenty percent. Such partial compression is shown in FIGS. 2-4 herein. Of further significance, slight deformation also occurs for the respective conductive layers 35 which are connected to the through-hole copper material. This deformation is represented by the bend-

ing shown in FIGS. 2-4 for the two conductive layers connected to a respective through-hole. Despite such deformation, no significant adverse impact on these conductive layers, including at the location of connection with the respective through-holes, occurred.

As also seen in FIG. 2, partial embedding of the land segments of each through-hole occurred within the respective, adjacent surface of the dielectric. (It is noted that such embedding occurred in the upper surface of subassembly 20. This results from this upper surface being engaged by a platen or similar member during the compression process.) In comparing FIG. 2 to the graph on FIG. 5, the compression step at FIG. 2 occurs at the location represented by the letter "A". As further seen in FIG. 2, no diffusion of the various metals which form part of the defined through-holes has occurred at this initial stage.

In the next step, as shown in FIG. 3, the compressed subassemblies are heated to a temperature, significantly, above that of the eutectic (first alloy) melting point of the gold and tin metal layers. This occurs at the aforementioned pressure of 300 psi but below the melting point of the dielectric PTFE material 40. As a result, the gold and tin layers at least partially melt (as shown) to form what can be referred to as a first alloy of these two metals. In a preferred embodiment, these subassemblies were heated to a temperature of about 280° C. to about 320° C. for a period of about 20 minutes to about 80 minutes. As stated, this is below the melting point of the PTFE dielectric, determined to be about 330° C. A preferred time for this extended heating is 60 minutes. In addition to the gold-tin alloy as defined, partial diffusion of the underlying copper into this alloy may occur at this stage. This first alloy is represented by the new-cross-hatching in FIG. 3 and identified by the numeral 71. In comparing FIG. 3 to FIG. 5, the step shown in FIG. 3 can be represented by the letter "B" in FIG. 5. As shown in FIG. 5, this structure has now exceeded the melting point of this first alloy but is less than the designated melting point of the dielectric. In FIG. 5, these heated and compressed subassemblies are shown as being retained at the above temperature and pressure for a time period of about 20 minutes, or a total period of approximately 70 minutes from the time of initial heating. Heating at this pressure assures continual diffusion of the copper into the gold-tin alloy to form what can be referred to as a second alloy of the three metals. Importantly, this new alloy possesses a melting point substantially greater than that of the dielectric and of the first alloy. This second alloy melting point is illustrated in FIG. 5. In the embodiment defined above, using the metals and respective thickness defined, this new melting point was determined to be above 390° C. Most importantly, this new alloy solidifies to form a permanent metallurgical bond between the respective pairs of throughholes. As further seen in FIG. 3, each of the respective land portions 53 are substantially fully embedded within the respective dielectric surfaces.

During the aforementioned step, use of a through-hole of hollow configuration provides an added benefit. Specifically, excess liquid metal, if present, will flow inwardly of the cylindrical body and not in an outward direction (which could result in possible bridging to an adjacent bonding surface).

In the next step of the invention, as shown in FIG. 4, the compressed subassemblies are subjected to increased temperature for the purpose of melting the dielectric to finalize the bond between the two assemblies. This occurs at a pressure of 300 psi. In a preferred embodiment, the subassemblies were heated to a temperature of about 330° C. to about 390° C., above the approximate 330° C. melting point for the dielectric PTFE. In one example, this temperature was 380° C., the subassemblies held at said temperature for about 30 migrates. Significantly, this temperature is below the melting point of the gold-tin-copper (second) alloy, which alloy will thus remain solid and thereby prevent incursion of melted dielectric therein. Such incursion could adversely affect the electrical connection between the respective through-holes. This second alloy is shown in FIG. 4 by the cross-hatching identified by the numeral 73. As seen, a substantially solid bond occurs between the respective facing land surfaces of each through-hole. Further, this new alloy is shown to extend downwardly along the internal surfaces of the lower through-hole. In the illustrated embodiment, such alloy formation is not seen to occur along the inner surfaces of the upper through-hole, wherein the aforementioned second metal (tin) was not utilized. The previous line of demarcation between the two subassemblies is partially removed in FIG. 4 to illustrate the substantial homogeneous bonding between the respective dielectric materials in these now fully bonded subassemblies.

The step shown in FIG. 4 can be represented by the letter "C" in FIG. 5.

Following this heating of the compressed subassemblies, the bonded subassemblies are then cooled at a predetermined rate, such cooling occurring at the 300 psi pressure maintained continuously throughout the process defined herein. In a preferred embodiment, cooling occurred at a rate of about 2° C. per minute until a temperature of about 260° C. was reached, following which accelerated cooling was accomplished. This cooling occurred using known equipment and processes, and further description is not believed necessary.

Finally, with the newly formed multilayered structure fully bonded, the applied pressure (300 psi) was removed.

The two subassemblies formed in accordance with the teachings described above may now be utilized as a multilayered circuit board assembly. Alternatively, such subassemblies may be combined with other subassemblies and treated in accordance with the teachings herein to form an even larger structure. The teachings herein may be used to produce printed circuit boards of conventional external (width and length) dimensions as well as those of much greater or lesser dimensions.

Thus, there has been shown and described a process for making a multilayered circuit board assembly wherein individual layered subassemblies are uniquely bonded together in such a manner that effective electrical coupling between respective pairs of through-holes thereof occurs. The method as defined herein possesses at least two unique features: (1) the use of compressible through-holes which assure effective engagement between respective pairs of such elements in structures utilizing several thereof, as is typically required; and (2) a dual heating step wherein the compressed subassemblies are initially heated to below the dielectric melting point for a predetermined time period to assure formation of an alloy having a melting point significantly greater than that of the dielectric, thereby permitting subsequent elevated heating of the compressed subassemblies to above the dielectric melting point. The lat-

ter feature is considered particularly noteworthy because the formed bond between the respective through-holes substantially prevents melted dielectric from incursion therein, which could adversely affect the formed bond between these conductive elements. Significantly, the invention substantially eliminates this from occurring to result in an end product of high integrity.

While there have been shown and described what are at present considered embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications can be made therein without departing from the scope of the invention as defined by the appended claims.

What is claimed is:

1. In a multilayered circuit board including at least two layered subassemblies each including at least one dielectric layer having opposing surfaces, electrically conductive wiring in the form of at least one conductive layer, and at least one conductive through-hole therein having a cylindrical portion and opposing land segments, the improvement wherein said layered subassemblies are aligned and engage one another, one of said land segments of said through-hole of one of said layered subassemblies engaging and being bonded to one of said land segments of said through-hole of another of said layered subassemblies, said bonded through-holes being of compressed shape such that the side walls of said cylindrical portions of said compressed through-holes are of substantially curved configuration.

2. The improvement of claim 1 wherein said cylindrical portions of said bonded through-holes are hollow.

3. The improvement of claim 2 wherein said side walls of said bonded through-holes are of a thickness of from about 0.2 mil to about 1.0 mil.

4. The improvement of claim 2 wherein said cylindrical portions of said bonded through-holes each have an external diameter of from about 3 mils to about 10 mils.

5. The improvement of claim 2 wherein said bonded through-holes are comprised of copper.

6. The improvement of claim 2 wherein each of said land segments of said bonded through-holes are substantially fully embedded within a respective, adjacent one of said opposing surfaces of said dielectric layer.

7. The improvement of claim 2 wherein each of said conductive layers of said electrically conductive wiring is connected to a respective one of said bonded through-holes, said conductive layers being of bent configuration.

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PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 24 August 2000 (24.08.00)	
International application No. PCT/US99/20418	**Applicant's or agent's file reference** 5687-009
International filing date (day/month/year) 07 September 1999 (07.09.99)	**Priority date** (day/month/year) 10 September 1998 (10.09.98)
Applicant COTTON, Martin, A.	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

13 March 2000 (13.03.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Claudio Borton
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